# Auviz Systems Announces Video Content Analysis Platform for FPGA’s at Embedded Vision Summit

AuvizVCA accelerates application development by removing complexities of FPGA programming

Campbell, Ca., May 2, 2016 -Auviz Systems, a leader in Accelerating Algorithms on FPGA’s for Data Centers and Embedded Devices today announced the availability of a Video Content Analysis Platform, AuvizVCA. AuvizVCA utilizes Semantic Segmentation to perform fast, accurate image detection and classification for a wide range of end markets; it delivers real-time (more than 30 fps) performance for 2-21 classes of objects without requiring any knowledge of FPGA programming. AuvizVCA and other Auviz technologies will be demonstrated at the Technology Showcase during the [Embedded Vision Summit](http://www.embedded-vision.com/summit), May 2-3 at the Santa Clara Convention Center. In addition, company CEO, Nagesh Gupta will also give a presentation on AuvizVCA technology, *Semantic Segmentation for Scene Understanding: Algorithms and Implementations.*

Unlike object detectors and classifiers in traditional computer vision systems, AuvizVCA implements a Convolutional Neural Network to perform Semantic Segmentation and image classification. This approach accurately identifies and classifies multiple objects with real-time performance on still or video inputs. AuvizVCA can be quickly integrated into applications requiring image detection and classification such as Free Space Detection for Autonomous Vehicles or as a ‘Virtual Tripwire’ for Security and Surveillance.

AuvizVCA is implemented as an OpenCL kernel optimized for FPGA devices; it is invoked through high-level language calls on the host processor. AuvizVCA runs on a wide range of FPGA devices and is fully programmable.

During execution AuvizVCA invokes AuvizDNN, an optimized library of Deep Neural Network functions similar to CuDNN. AuvizDNN is fully programmable and can implement any type of network through an API without having to run the FPGA implementation tools. It supports deployment of DNN’s and is scalable to run on any type of FPGA device size and deliver the highest overall performance (latency, images/sec). AuvizVCA calls functions from AuvizDNN to implement its semantic segmentation approach.

AuvizVCA together with a COTS PCI-E accelerator board from Alpha Data (ADM-PCIE-7V3) and the Xilinx SDAccel run time environment provide a complete Image Detection and Classification Accelerator with performance more than 30 fps. Future versions of AuvizVCA will support other FPGA Accelerators and Ultrascale MPSoC and SOC-FPGA devices from Xilinx and Altera with higher levels of performance.

Demonstrations and presentations at the Embedded Vision Summit

In the Technology Showcase, Auviz Systems will be demonstrating AuvizVCA, AuvizDNN and two other libraries: AuvizCV, optimized OpenCV, and AuvizLA, optimized BLAS for FPGAs.

Nagesh Gupta, Founder & CEO of Auviz Systems will present how FPGAs can be used to accelerate image detection and classification on Tuesday May 2, 2016. The presentation titled “Semantic Segmentation for Scene Understanding: Algorithms and Implementation” describes some of the implementation details for AuvizVCA.

*“The use of machine learning for cloud computing is exploding, powering a diverse set of applications such as intelligent video surveillance and automatic editing of action-cam videos,” said* ***Jeff Bier, Founder of the Embedded Vision Alliance****.  “By enabling cloud developers to tap the parallel computing power of FPGAs – without having to delve into the complexities of FPGA programming – Auviz is lowering barriers to mass deployment of cost-effective, cloud-based visual intelligence.”*

**About Auviz Systems**

Auviz Systems is the technology leader in Accelerating Algorithms for FPGAs. For more information, visit [www.auvizsystems.com](http://www.auvizsystems.com/)

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