DRP* TECHNOLOGY ENABLES A HYBRID APPROACH FOR EMBEDDED VISION SOLUTIONS

* DYNAMICALLY RECONFIGURABLE PROCESSOR

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GREG LARA
SENIOR PRODUCT MARKETING MANAGER
COGNITIVE PRODUCTS DEPARTMENT
ENTERPRISE INFRASTRUCTURE BUSINESS DIVISION
RENESAS ELECTRONICS CORPORATION

AGENDA

- Renesas introduction
- The Vision Processing Challenge
- Dynamic Reconfigurable Processor (DRP) Technology Overview
- RZ/A2M MPU with DRP Technology
- DRP Application Solutions
- Design Resources for RZ/A2M MPU with DRP Technology

WHO WE ARE

THE WORLD'S LEADING EMBEDDED SOLUTION PROVIDER

Originating from Hitachi, Mitsubishi, NEC, and Intersil
Net sales 757.4 billion yen in 2018
19,000+ employees worldwide
Headquartered in Tokyo, Japan

2002 NEC Electronics
Spin-off from NEC

2003 Renesas Technology
Spin-off from Hitachi and Mitsubishi merger

2010 Renesas Electronics started operation
NEC Electronics and Renesas Technology merged

2017 Acquisition of Intersil
Strengthen leadership in the analog market

2019 Acquisition of IDT
Integrated Device Technology: the leading supplier of analog mixed-signal products including sensors, connectivity and wireless power

RENESAS BROAD PRODUCT PORTFOLIO

Microcontrollers and Microprocessors

RL78 — 8/16-bit Ultra-Low Energy MCU
Sensing and Motor Control

RX — 32-bit High Power Efficiency MCU
Motor Control

RA — 32-bit Arm® Cortex®-M MCU
Advanced Security,
Connectivity & Flexible SW

RZ — 32/64-bit Arm®-based High-End MPU
Human Machine Interface, AI Inferencing
Industrial Network & Real-time Control

RE — SOTB™ Process-based
Energy Harvesting Embedded Controller
Battery maintenance-free IoT devices

RH850 — Renesas 40nm process MCU
Automotive only
Rich functional safety and security features

Analog & Mixed Signal, Power Discrete

- Analog Products
- Battery Management IC
- Clock & Timing, Digital Logic
- Interface & Connectivity
- Memory
- Optoelectronics
- Power Devices
- RF Products
- Sensor Products
- Space & Harsh Environment
- Video & Display IC
- Wireless Power

…and more

SoC, Integrated Platforms

R-Car — Automotive

R-IN — Factory automation

Renesas autonomy™ — Automotive

Renesas RZ/G Linux — Industrial, HMI

Renesas Synergy™ — IoT and IIoT

THE VISION PROCESSING CHALLENGE

IMAGE PROCESSING MARKET DYNAMICS

VISION EVOLUTION DRIVES NEED FOR MORE COMPUTING POWER AND CONNECTIVITY BANDWIDTH

EMBEDDED VISION PROCESSING DESIGN GOALS

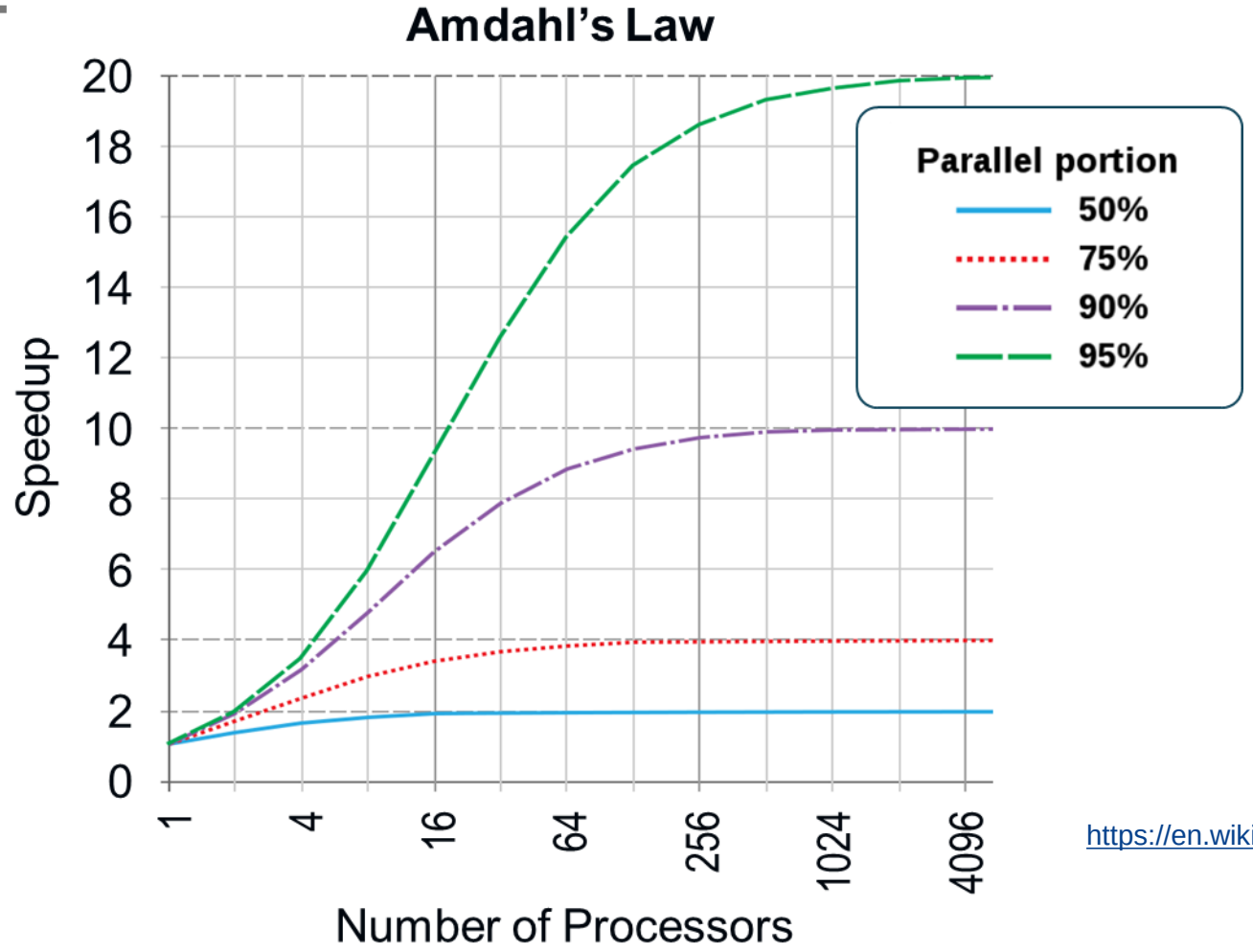
- **High performance**
  - More pixels
  - Higher frame rates
- **Low power consumption**
  - Battery powered operation
  - Thermal dissipation
- **Small form factor**
  - Hand held
  - Sealed enclosures
- **Low cost**
  - BOM complexity
  - Manufacturing complexity
- **Fast time to market**
  - Flexible design

EXISTING ARCHITECTURES

- **Software + Processor**
  - Multi-core
  - Faster clock
- **Hard IP**
  - Dedicated hardware
  - Optimized circuit
- **FPGA**
  - Field programmable hardware
  - Pipelined peformance

MULTI PROCESSOR PROBLEM: AMDAHL'S LAW

SPEEDUP IS LIMITED BY THE SERIAL PART OF THE PROGRAM

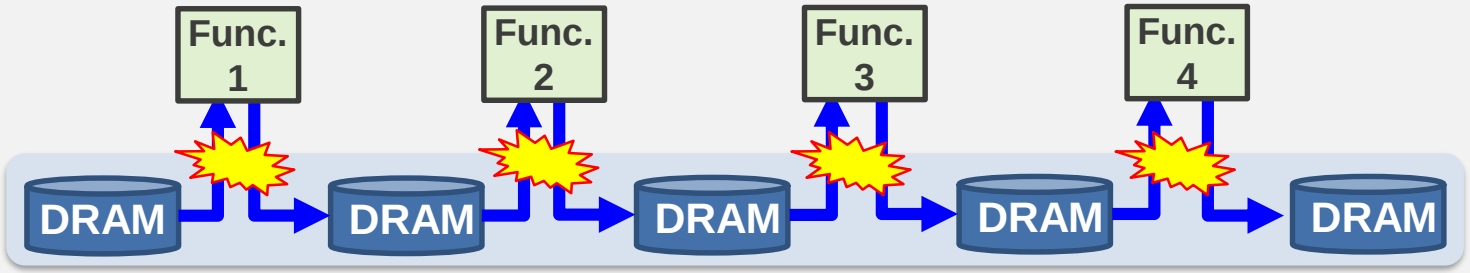


https://en.wikipedia.org/wiki/Amdahl%27s_law#

MULTI PROCESSOR PROBLEM: VON NEUMANN ARCHITECTURE

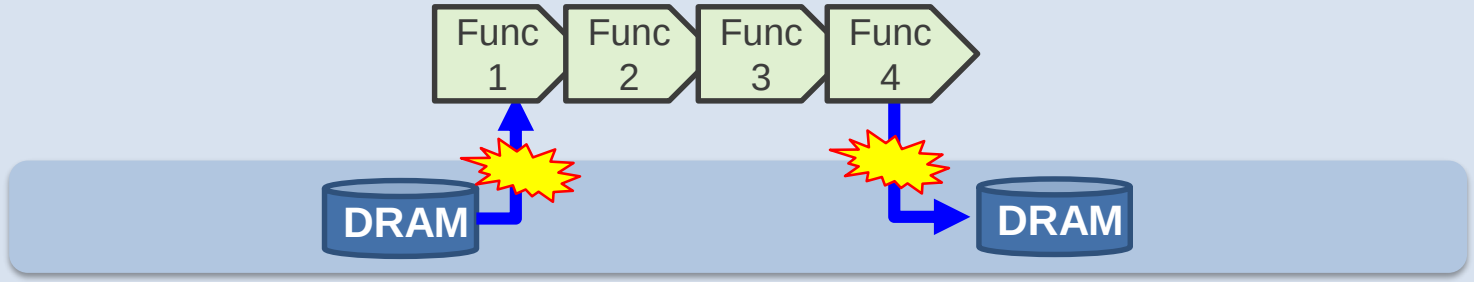
DATA TRANSFER DRIVES POWER CONSUMPTION

Conventional Software Implementation (CPU/DSP/GPU)

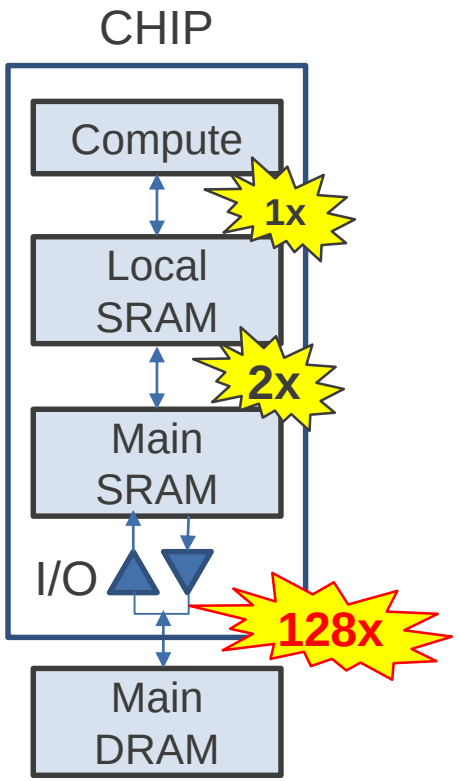


Sequential functions with many memory accesses
→ Consuming power with each data transfer

Wired Logic Architecture (ASIP/FPGA)



Saving memory access by combining multiple functions
→ Reducing power by minimizing memory access

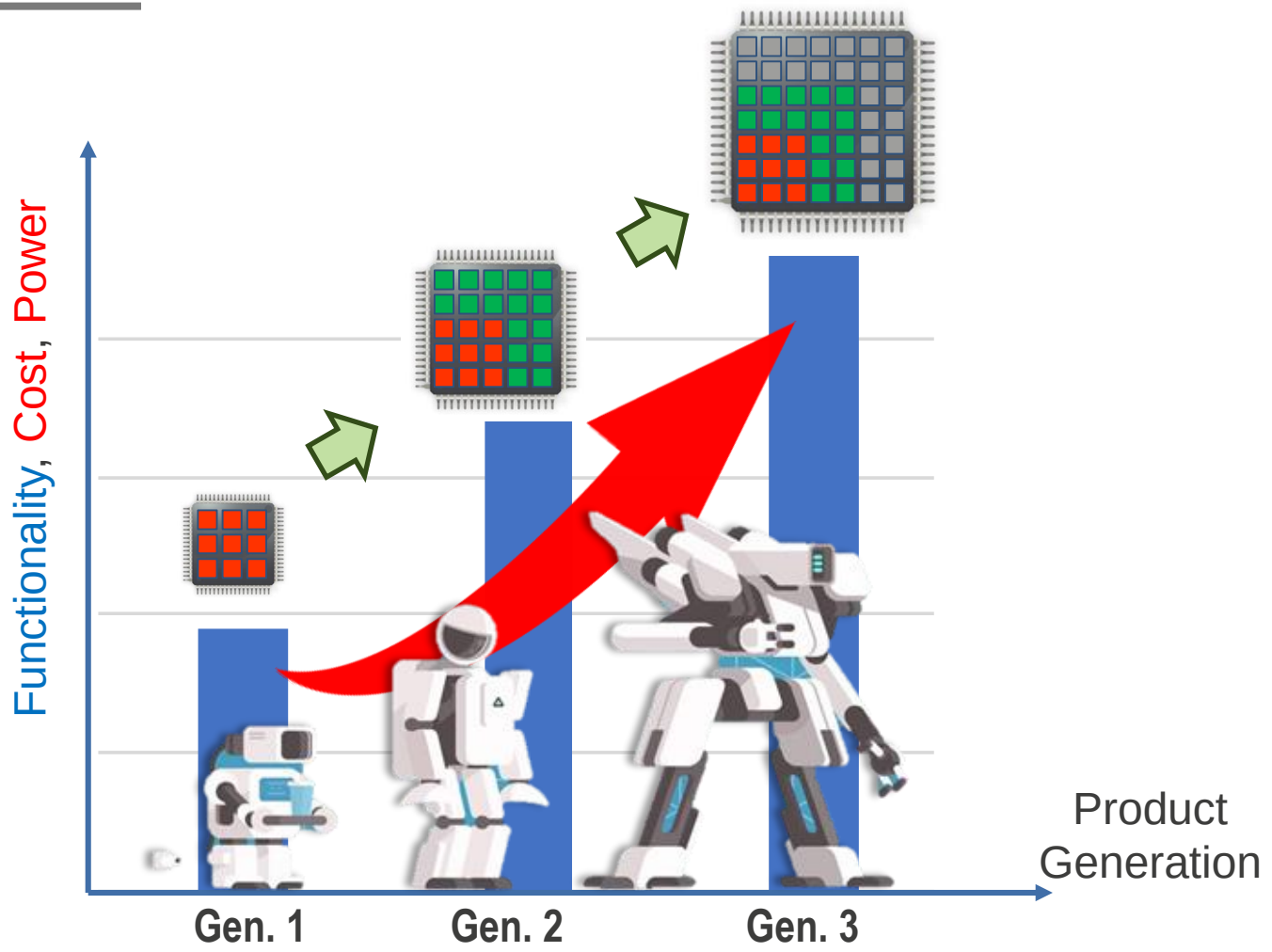


Relative energy consumption per equivalent MAC operation

Reference: presentation by Bert Moons

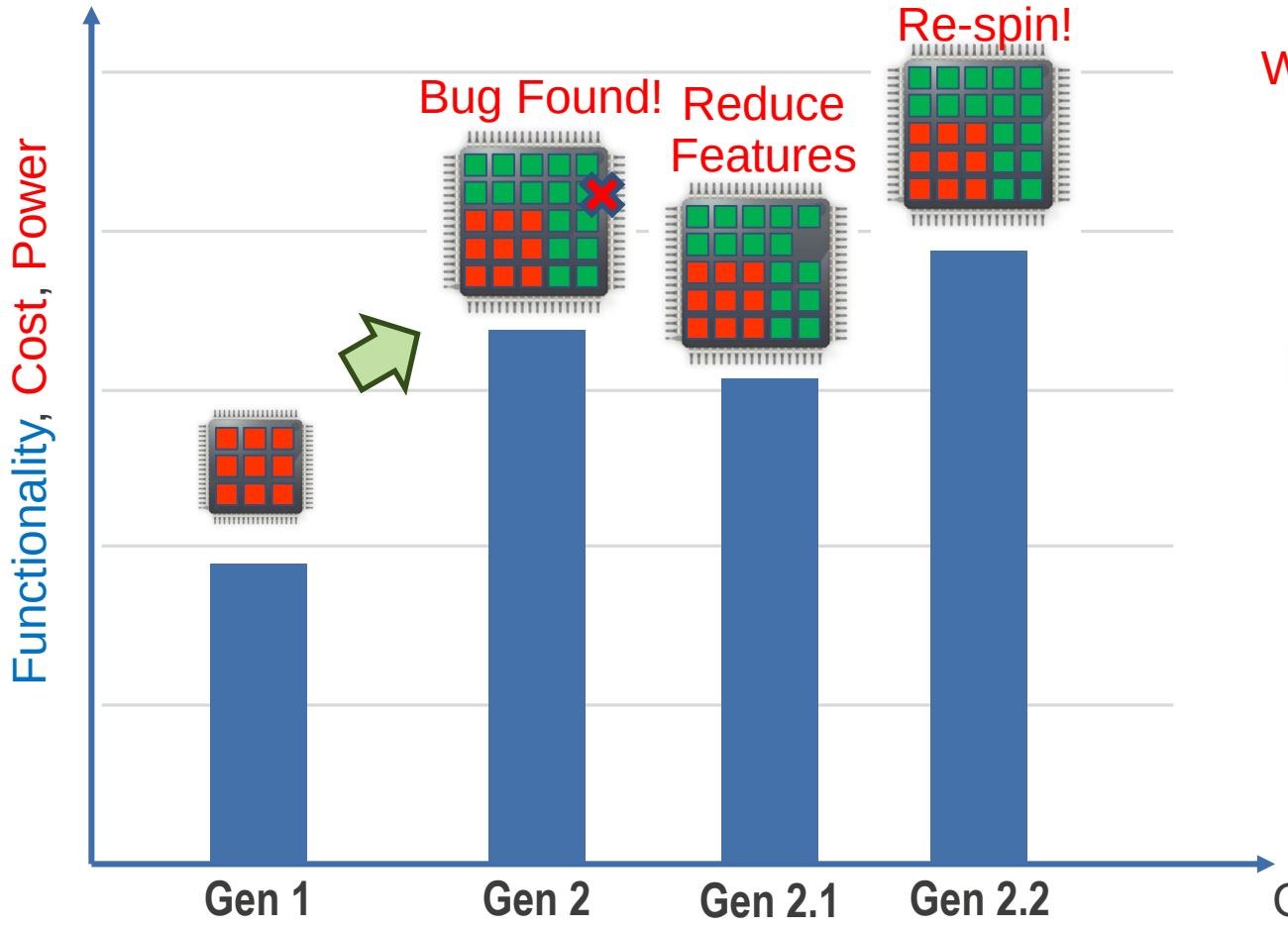
HARD IP TRADEOFF

FUNCTIONALITY INCREASE AT COST OF LARGER DIE SIZE AND POWER CONSUMPTION

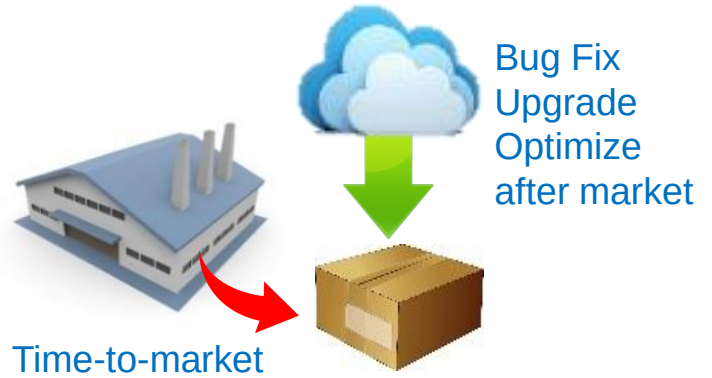


HARD IP LIMITATIONS

LIMITED FLEXIBILITY TO FIX BUGS FOR PRE-PRODUCTION AND MASS PRODUCTION



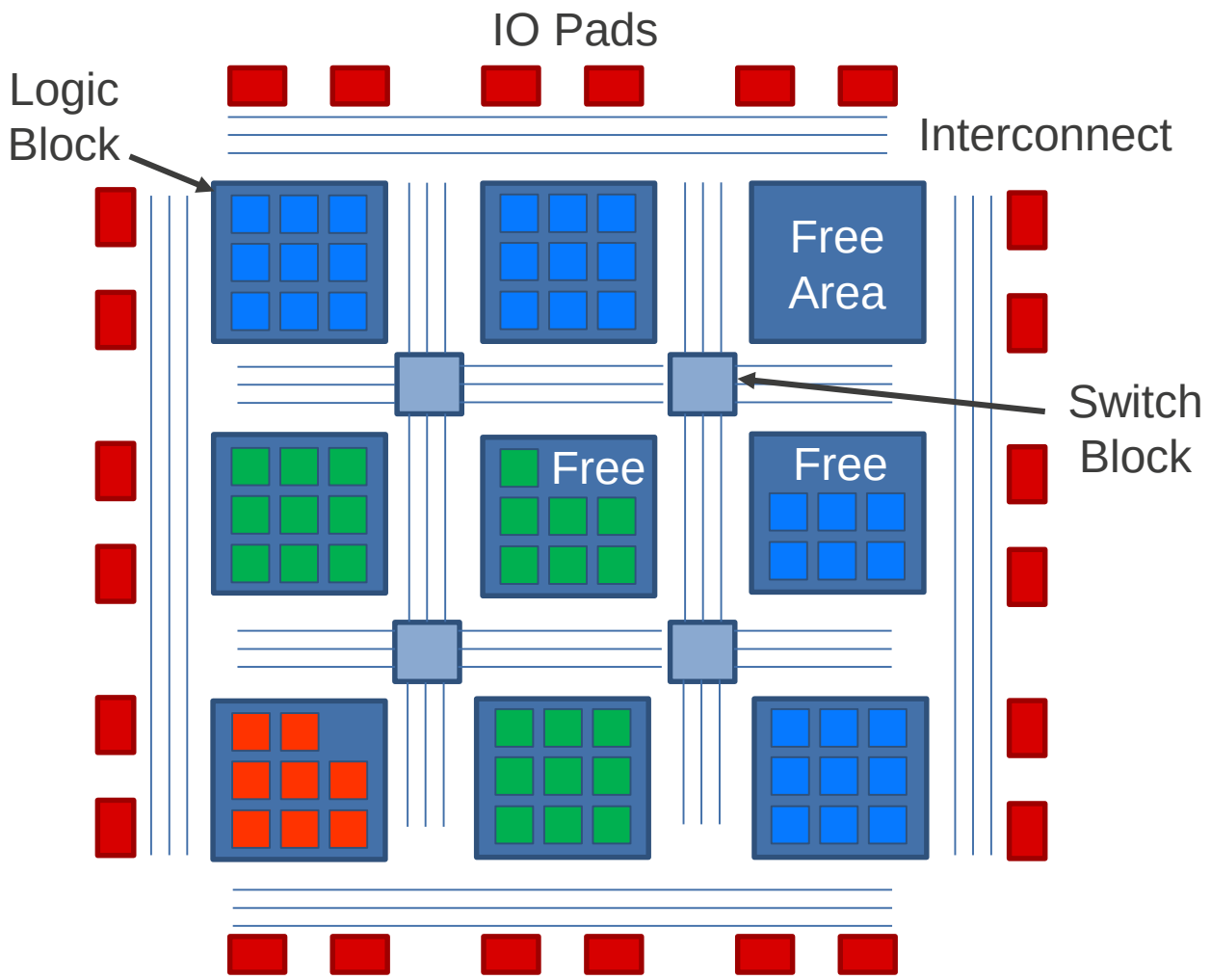
What if we find the bug in the field?



FPGA CHALLENGES

SILICON OVERHEAD, EFFICIENT MAPPING, SCALING

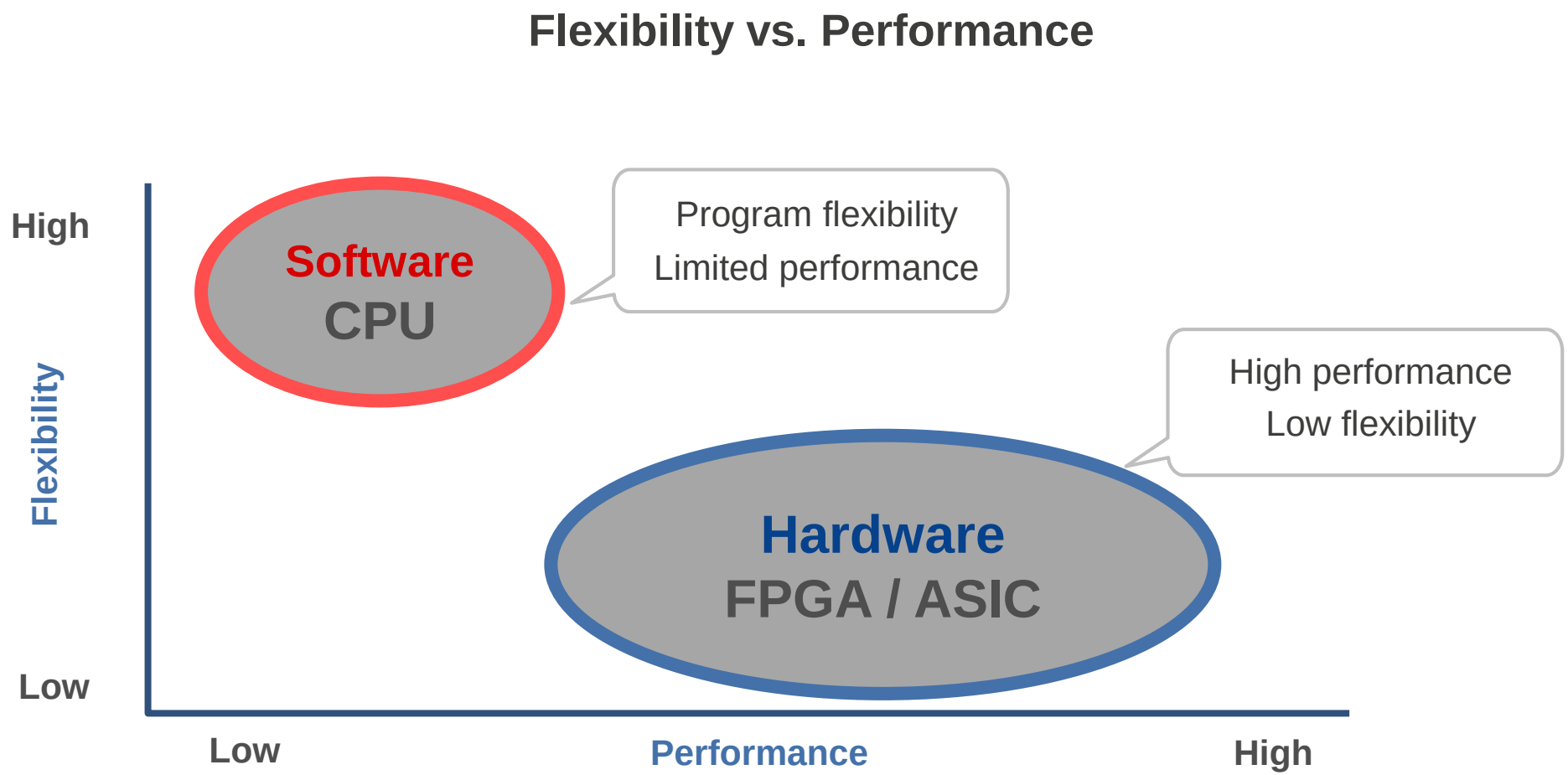
- Programmability requires tradeoff of increased die size, power, and cost
- Mapping design efficiently to FPGA resources is difficult
- Adding new features may force move to larger, more expensive, and power-hungry FPGA



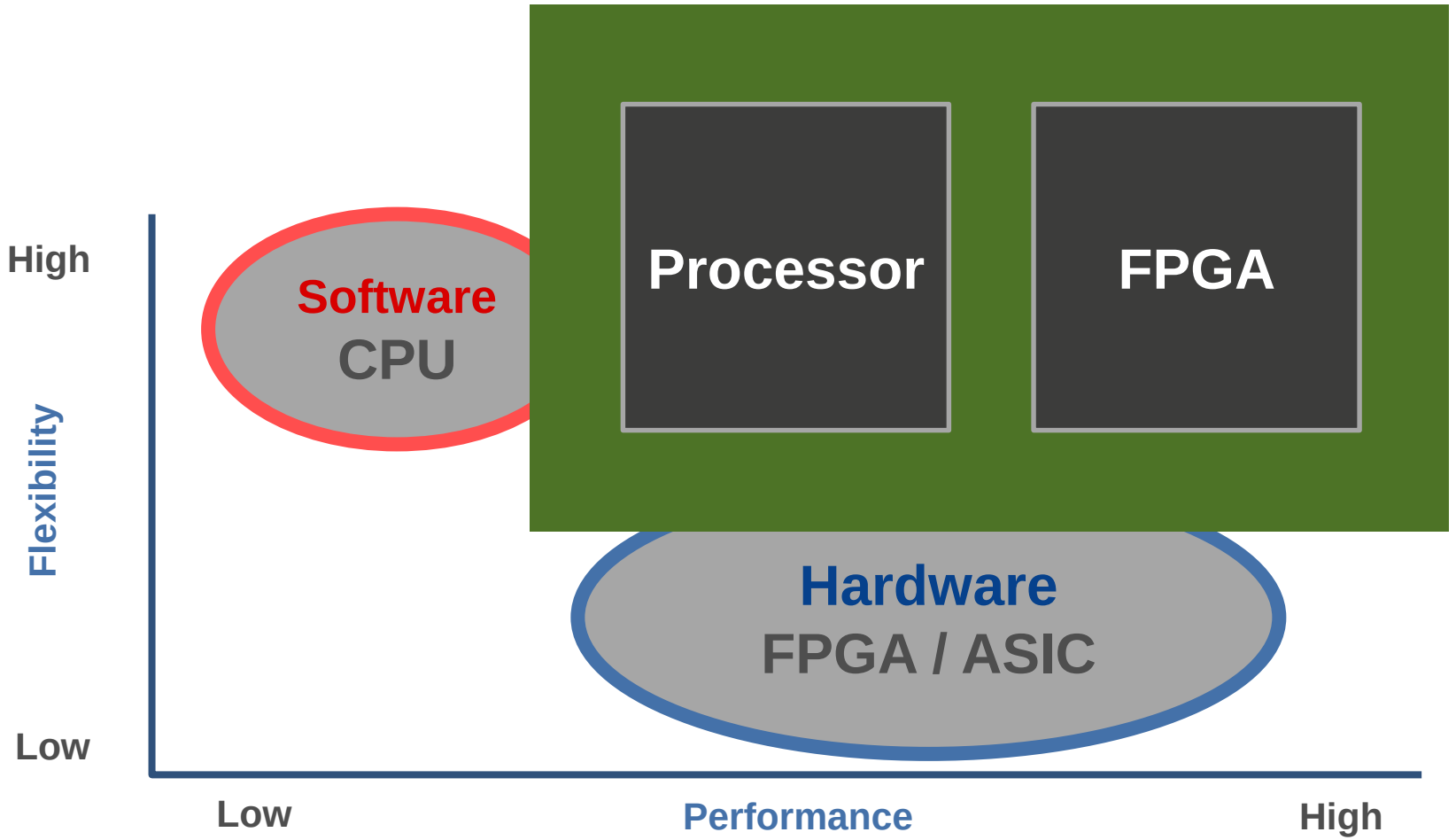
LIMITATIONS OF EXISTING ARCHITECTURES

- **Multi processor**
  - Limited scalability
  - Power hungry
- **Hard IP**
  - Adding functionality increases cost and power consumption
  - Not flexible
- **FPGA**
  - Power hungry
  - Area efficiency challenge

HARDWARE / SOFTWARE TRADEOFF



COMBINE PROCESSOR + FPGA?



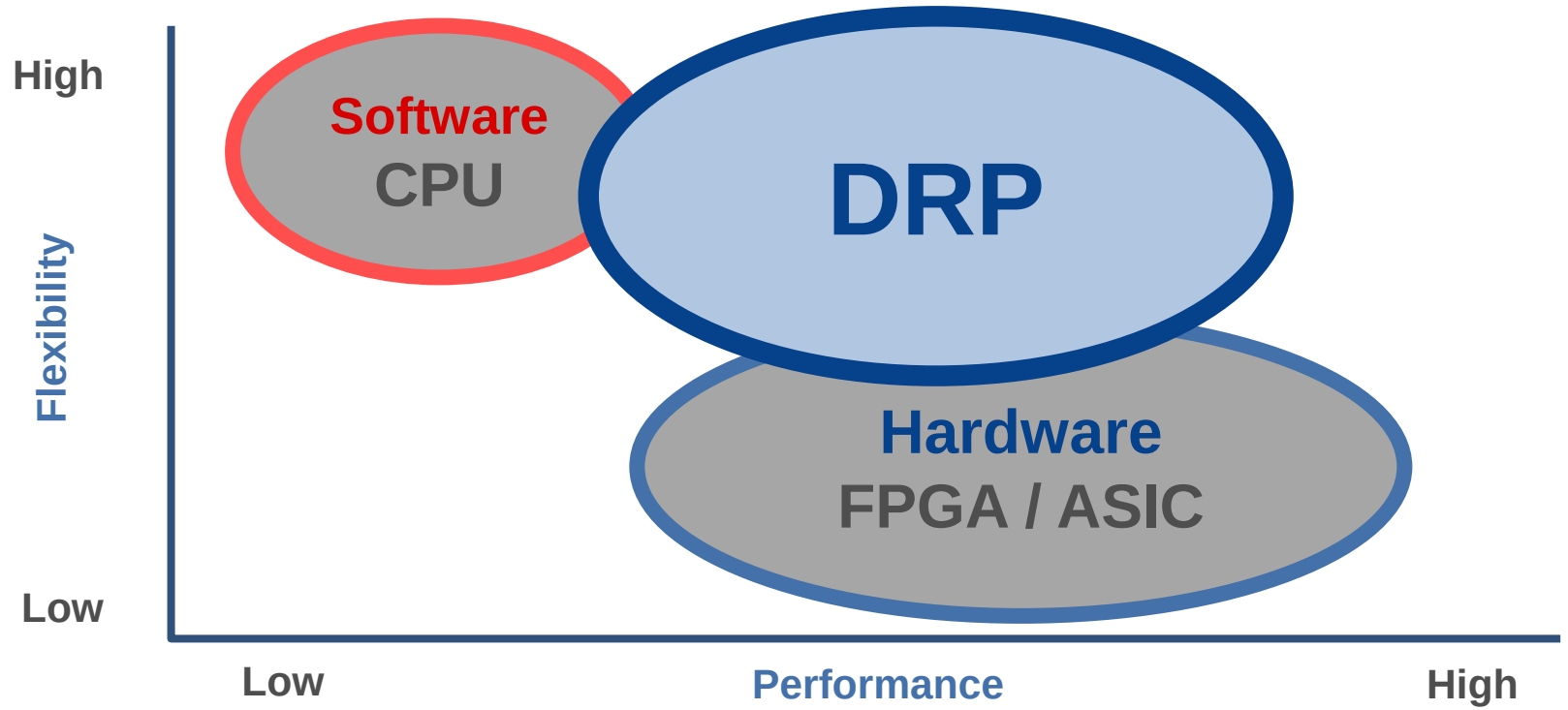
Penalty:

- Cost
- Power
- Heat
- Size
- Complexity

DYNAMICALLY RECONFIGURABLE PROCESSOR TECHNOLOGY

A Renesas Proprietary Accelerator Technology

Software Flexibility with Hardware Performance



DYNAMICALLY RECONFIGURABLE PROCESSOR TECHNOLOGY

Award Winning Technology
Recognized Around the World

December 2018
Electronic Products (US)
1st

April 2019
CITE (China)
1st

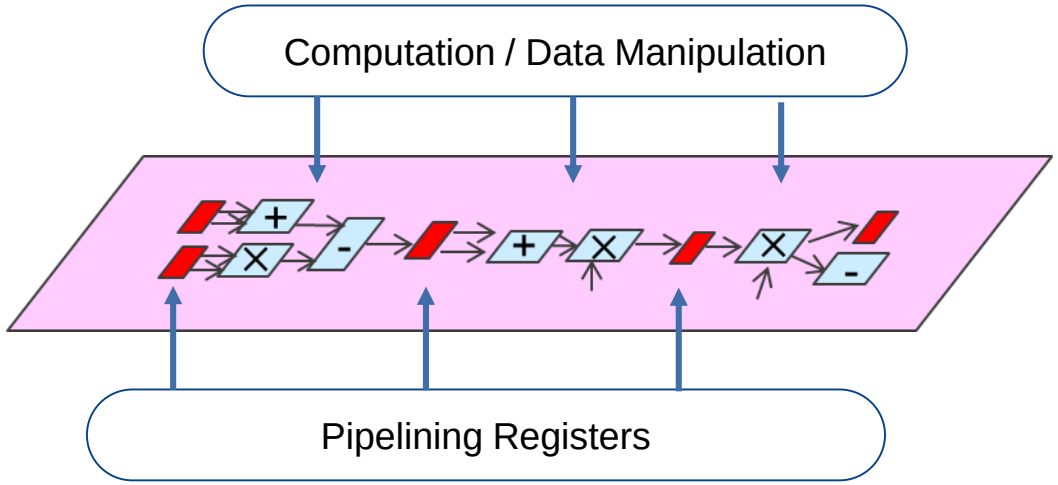
October 2019
Elettronica (Italy)
2nd

November 2019
Design World (US)
Silver

DRP TECHNOLOGY OVERVIEW

PIPELINED PROCESSING
SPATIALLY EXPANDED DATA PATH

FPGA

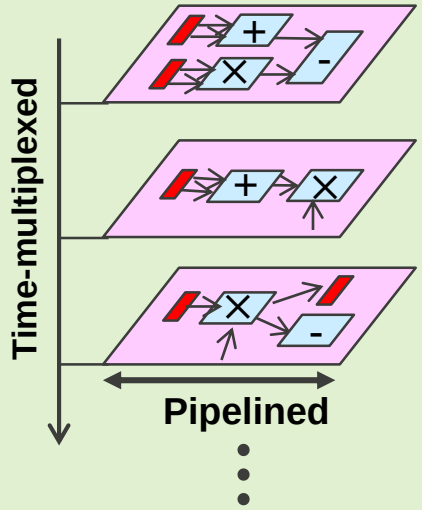


Pipelined processing

Spatially expand various operations into LUT architecture

High performance but large die area due to expansion

DRP

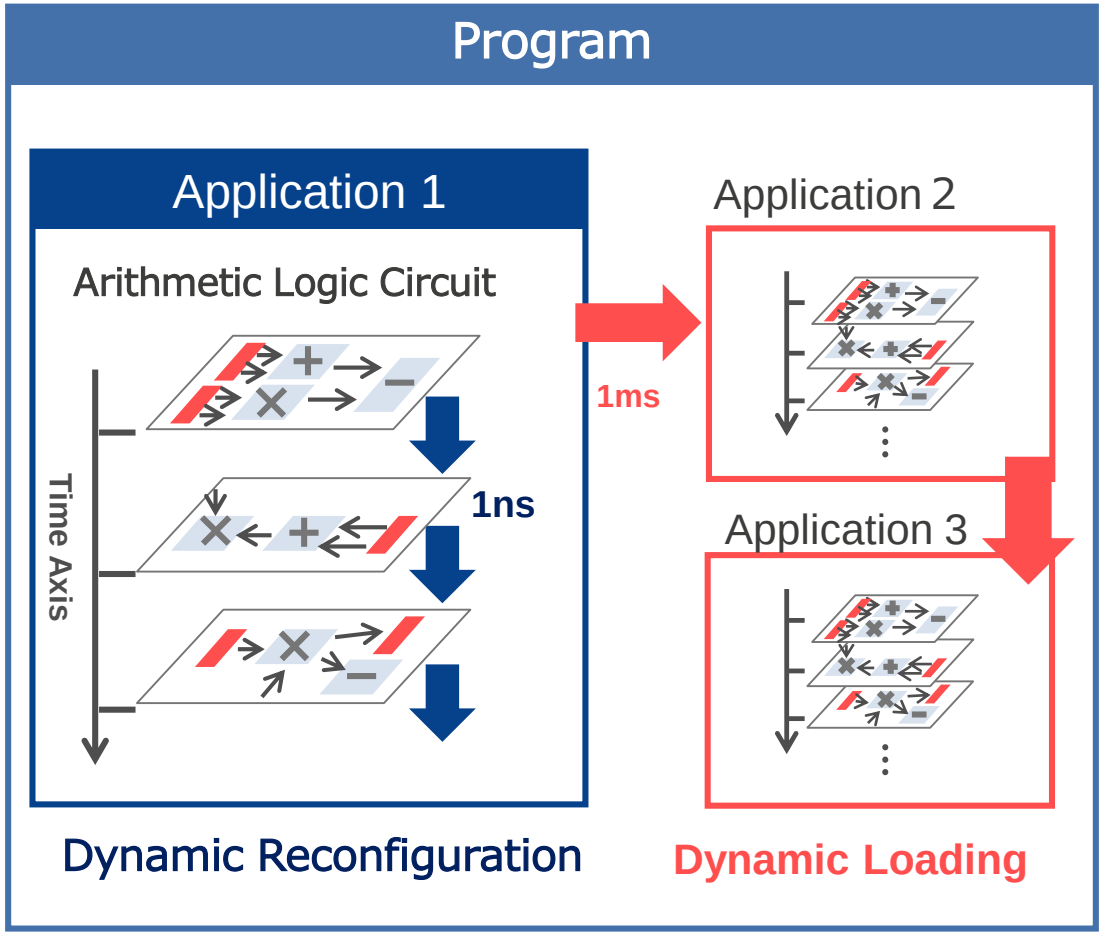


Process spatially expanded operations

High performance with area efficiency via **Dynamic Reconfiguration**

DYNAMICALLY RECONFIGURABLE PROCESSOR TECHNOLOGY

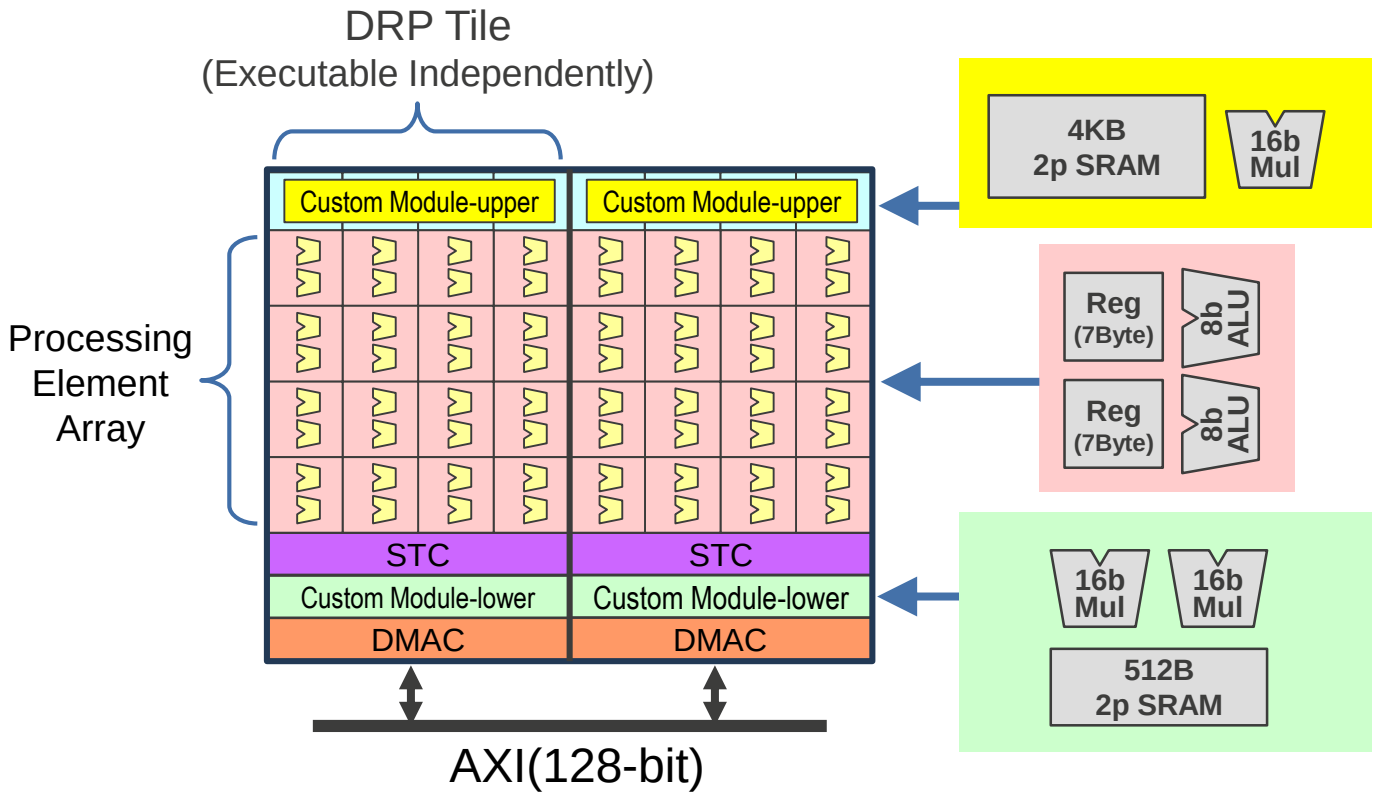
- Spatially expanded time-multiplexed data path
- Hardware IP (Intellectual Property) that can dynamically change its configuration
  - Reduce die area
  - Reduce power consumption
  - Deliver high performance
- **Dynamic Reconfiguration changes the configuration of the arithmetic circuit in 1 ns**
- **Dynamic Loading switches applications in 1 ms**



DRP HARDWARE ARCHITECTURE

PE (Processor elements), SRAMs, ALUs, STC (state transition controller), and DMAC

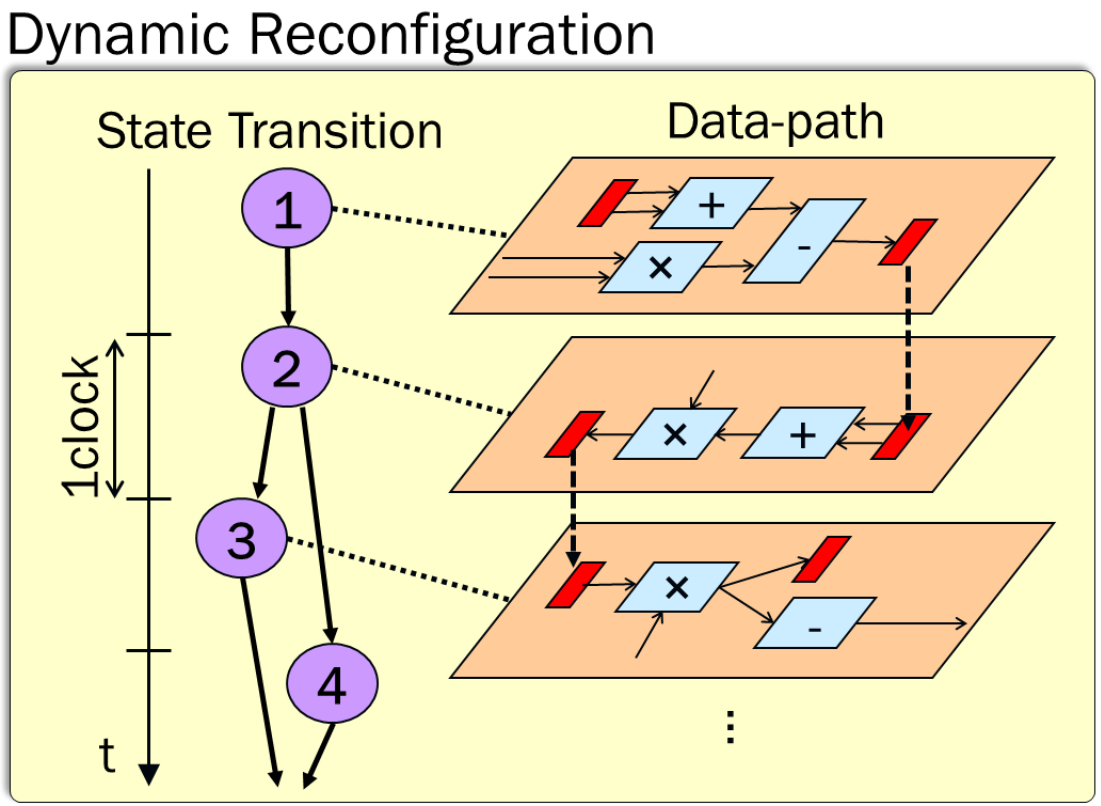
- Flexible coarse-grained reconfigurable architecture (Binary/8-bit)
- Tile-based scalability (48 PEs x 6 Tiles)
- Embedded Intelligent direct memory access controller (DMAC)



DYNAMIC RECONFIGURATION ARCHITECTURE

SPATIAL EXPANSION OF DATA PATH VIA TIME DOMAIN MULTIPLEXING

- Algorithm data path divided into multiple “contexts”
- DRP resources configured by context data
- Context loading directed by state transition controller (STC)



The state defines the data-path structure, which can transition to a new configuration within one clock cycle

DRP PROGRAMMING METHODOLOGY

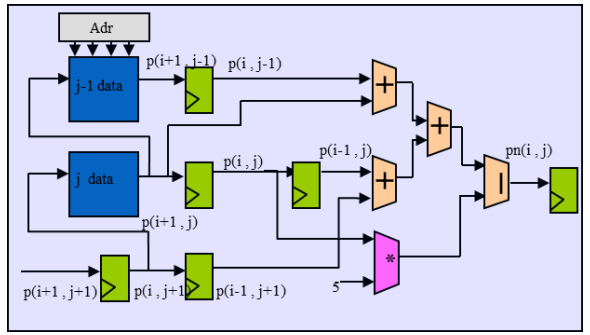
CREATING CUSTOM CONFIGURED HARDWARE ACCELERATOR

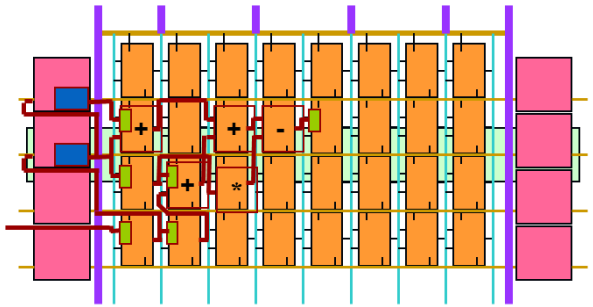
Algorithm expressed in C code

Dedicated Tool Flow
- Synthesis: C to HDL
- Mapping: HDL to DRP resources
- Placement and Routing

Binary for dynamically reconfigurable data path

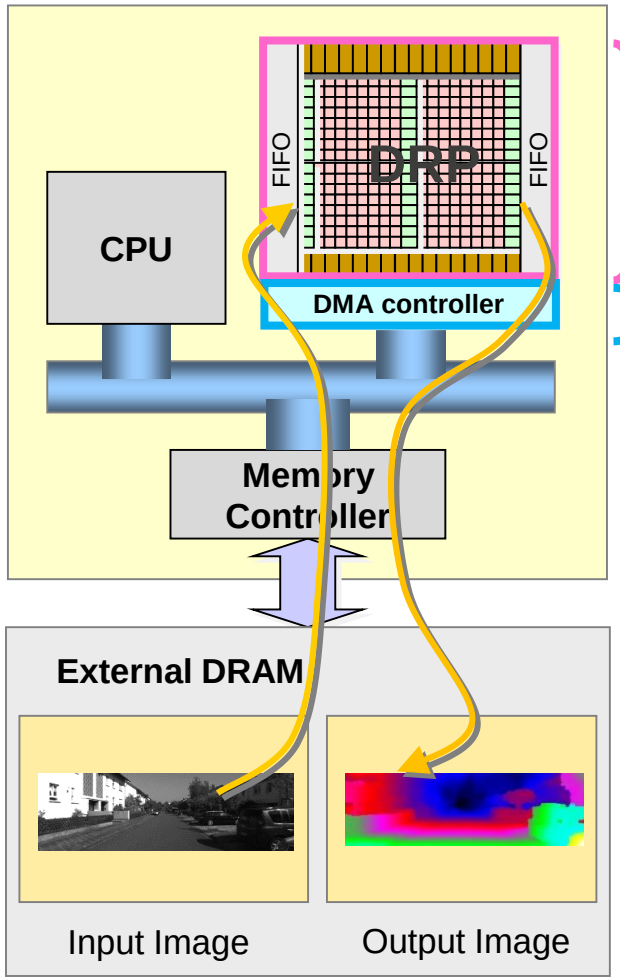
```
for( i = 0; i < N; i++ ){
     for( j = 0; j < N; j++){
          fn(i, j) = 5*f(i, j) – f(i, j–1) – f(i–1, j)
                           – f(i+1, j) – f(i, j+1);
     }
}
```





DRP IN THE SYSTEM

RECONFIGURABLE ARRAY + FAST DMA



Reconfigurable Processing Elements Array

- Created pipelined hardware to accelerate algorithm
- Run complex algorithms by switching configurations within a nanosecond (up to 64 contexts)
- Programming with C language via high-level Synthesis tool

Reduce memory bandwidth and achieve low latency

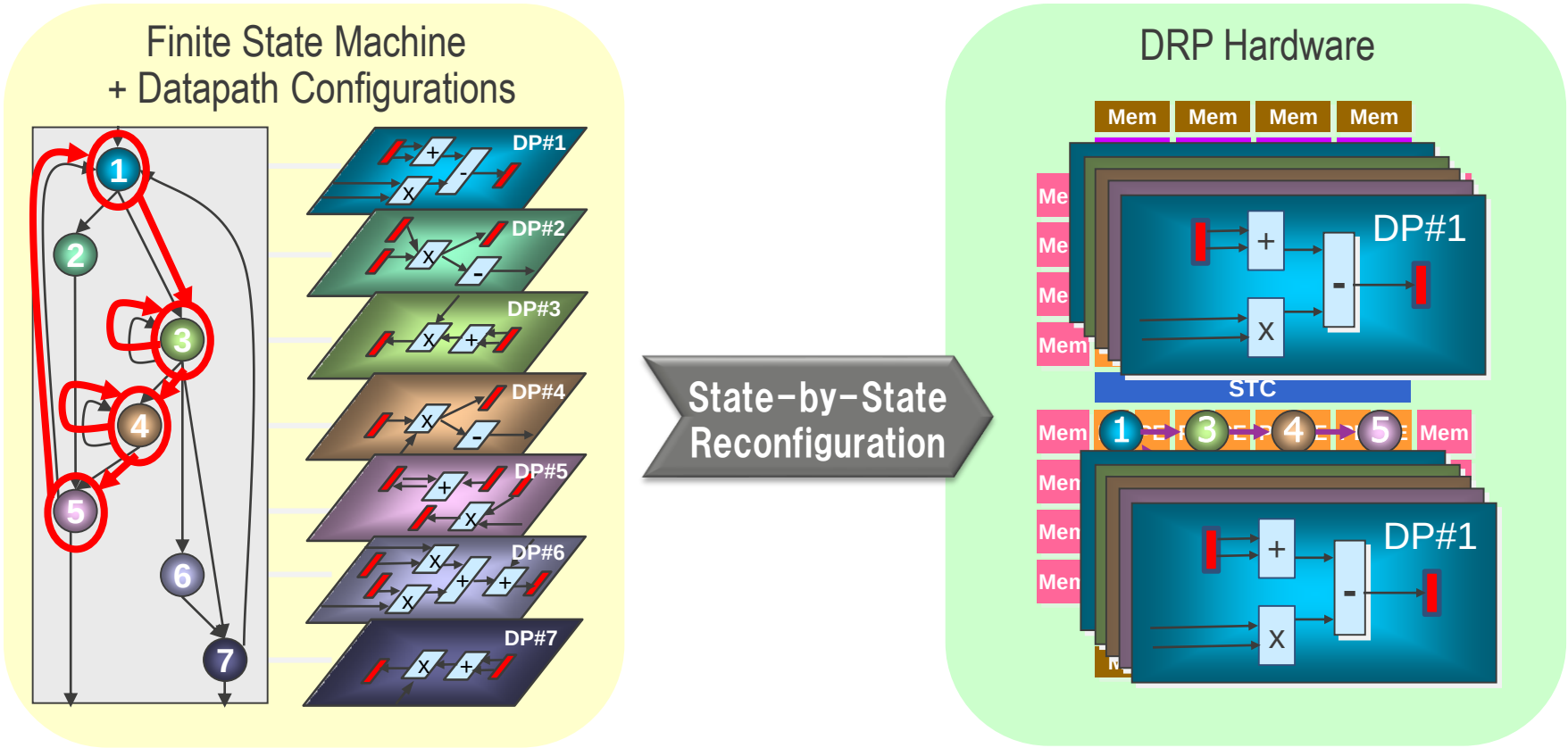
Fast and Intelligent Data Mover (DMA)

- Fast external memory access via integrated Direct Memory Access (DMA) controller
- C programming with access API
- Dynamic configuration loading in less 1ms from external memory

DYNAMIC RECONFIGURATION MECHANISM

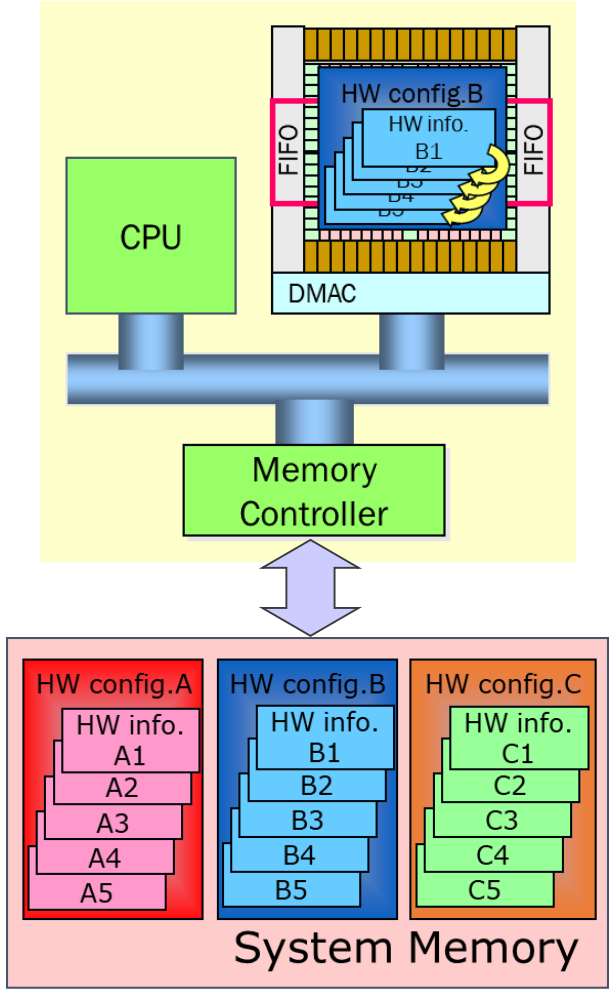
CYCLE-BASED DATA-PATH CONFIGURATION DIRECTED BY STC (STATE TRANSITION CONTROLLER)

Switch between multiple Data-paths with each DRP clock cycle to execute complex algorithms



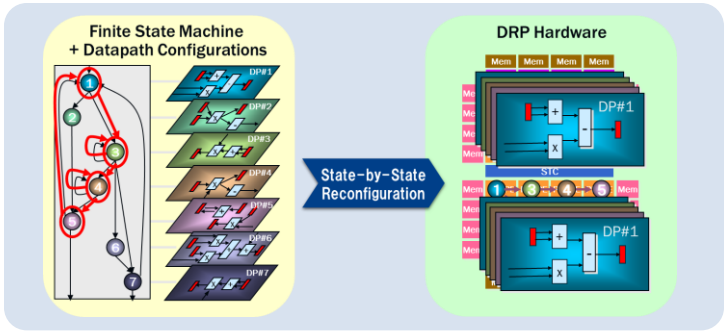
DYNAMIC LOADING TO SUPPORT MULTIPLE ALGORITHMS

SWITCH TO NEW ALGORITHM IN AS LITTLE AS ONE MILLISECOND



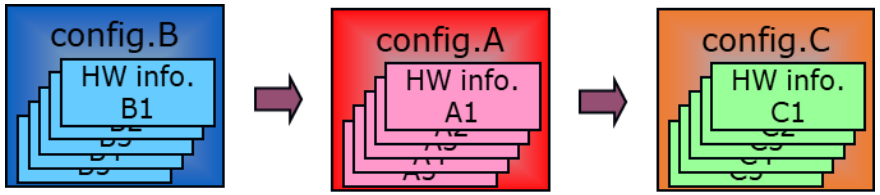
Dynamic reconfiguration in one DRP clock cycle

- Up to 64 contexts (HW configurations) stored in DRP
- Context switching managed by State Machine Controller



Dynamic loading of new configuration in <u>as little as 1 ms</u>

- Loads from external memory without interrupting execution
- Change to HW with completely different function set
- Time division execution of huge applications



DRP LIBRARIES

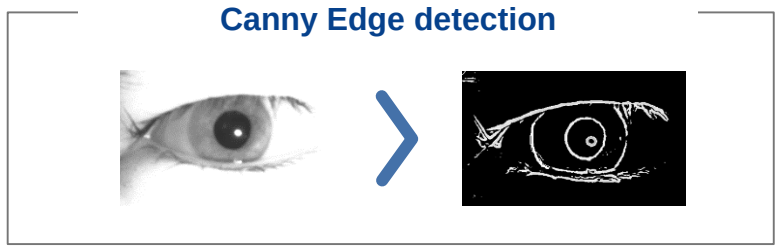
CURRENTLY MORE THAN THIRTY FUNCTIONS AVAILABLE AND MORE ON THE WAY

Real Time Camera Image Processing

- Color conversion
- Image filtering
- Geometric transformations
- Image enhancement

Image Recognition

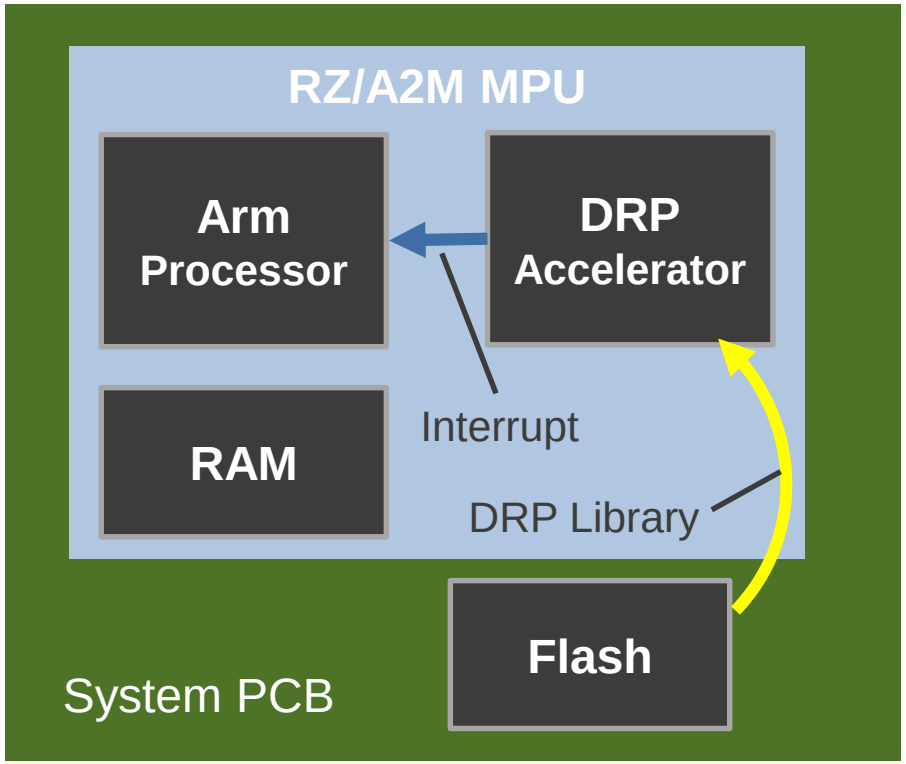
- Feature detection
- Morphological Transformation
- Other (Reed-Solomon error correction)



USING DRP LIBRARIES
SIMILAR TO USING A DRIVER API

- DRP is on-chip hardware accelerator
- Arm and DRP share system memory
- DRP library incorporated into application code like a driver API
- At run time, DRP:
  - Loads library binaries from Flash (or RAM)
  - Reads data from Input Address
  - Writes data to Output Address
  - Issues interrupt service request (ISR) to Arm processor when task is finished

```
Program code
.
.
DRP_Load [Library Address|
DRP_Activate
DRP_Start [Input_Addr, Output_Addr, etc.]
.
```



DRP TECHNOLOGY ENABLES REAL TIME IMAGE PROCESSING

Example Algorithm: Harris Corner Detection boosted 20 X!

Execution Time	
CPU*	235.3 ms
DRP	11.6 ms

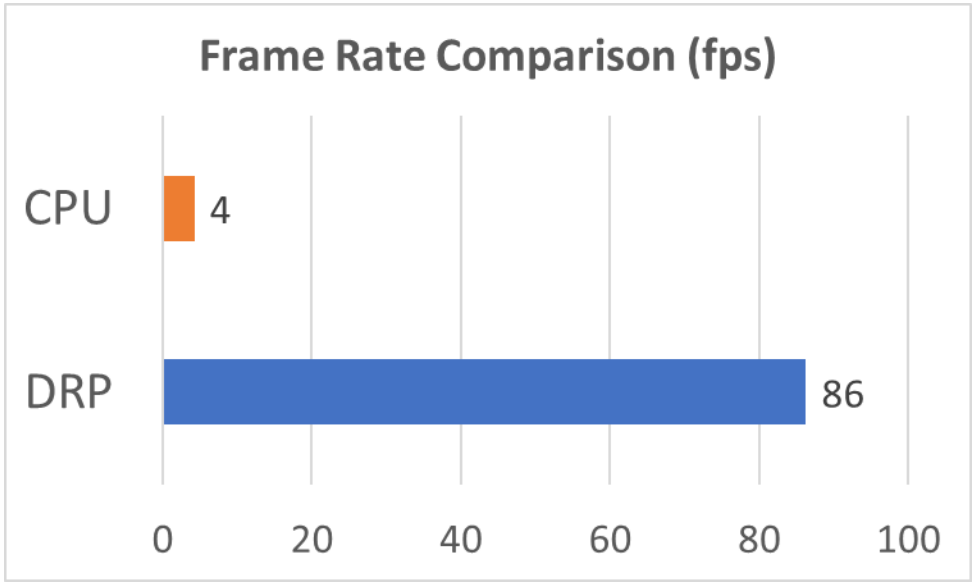


Image size : 640 x 480 VGA
Image Color : Grayscale 8BPP
CPU : RZ/A2M Cortex-A9 @528 MHz
DRP : max.66 MHz

* Using Open CV library

DYNAMIC LOADING IN MILLISECONDS

ACCELERATE SEQUENTIAL ALGORITHMS / PARALLEL PROCESSING ACROSS MULTIPLE DRP SLICES

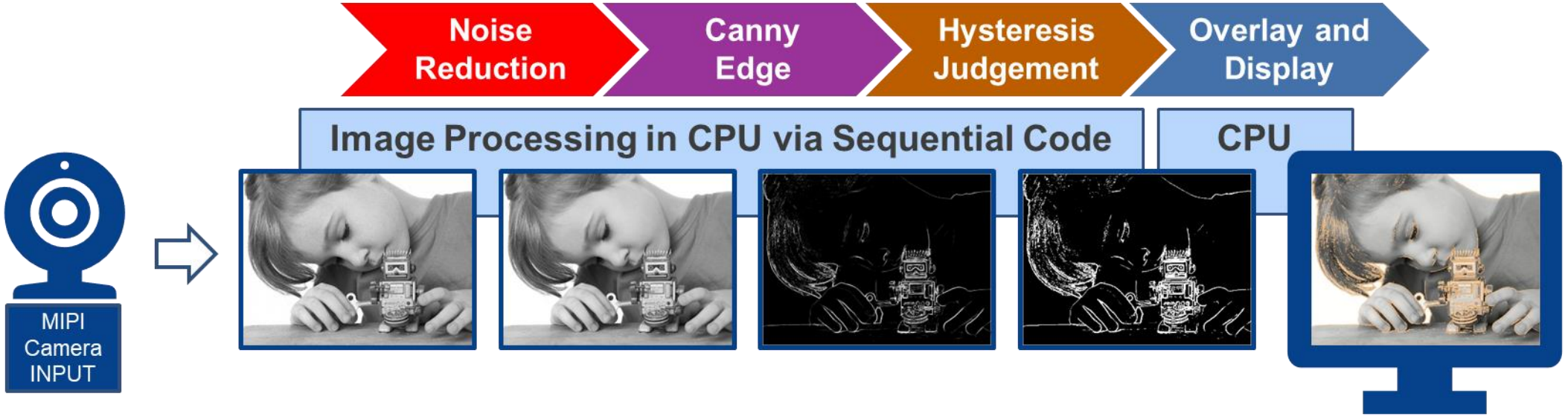


Image: 640x480 VGA, Grayscale 8BPP
CPU: RZ/A2M Cortex-A9 @ 528 MHz
DRP: 66MHz (max)

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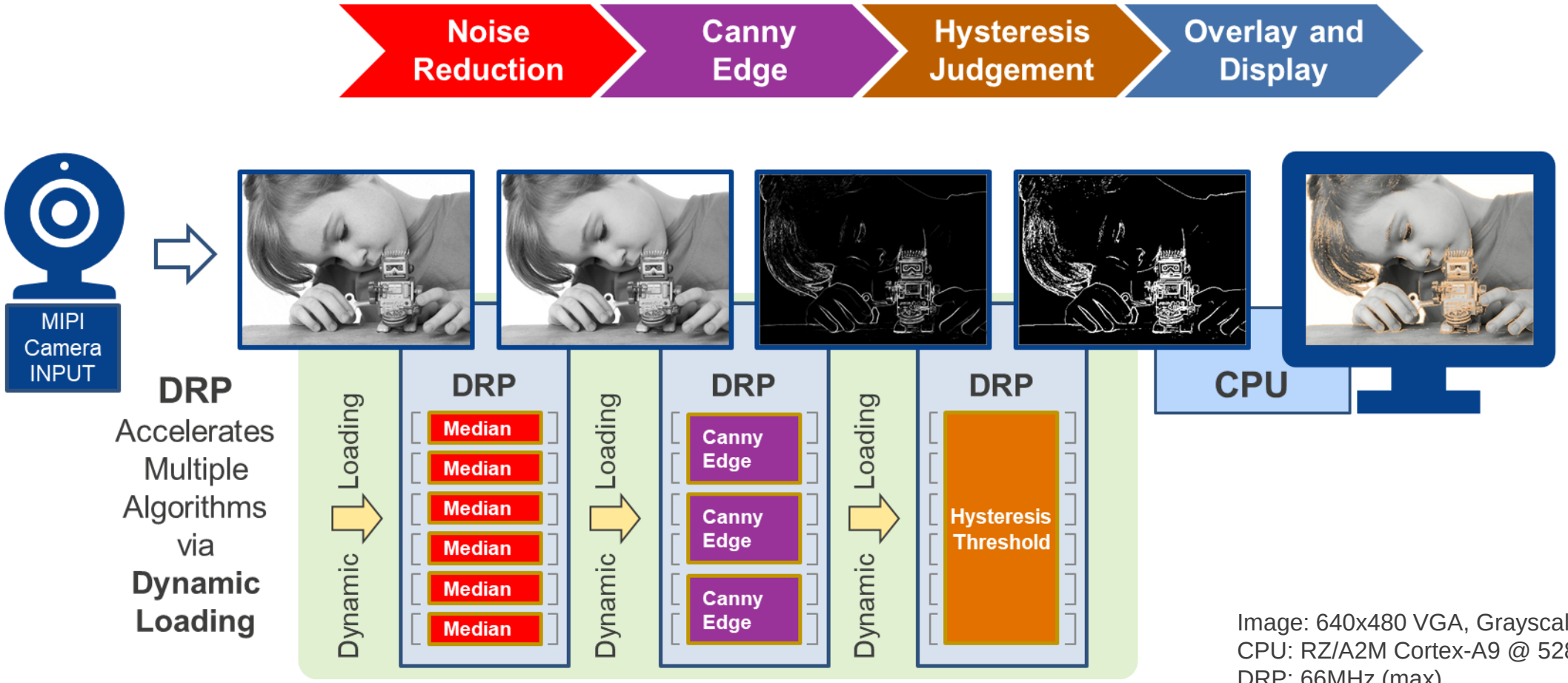

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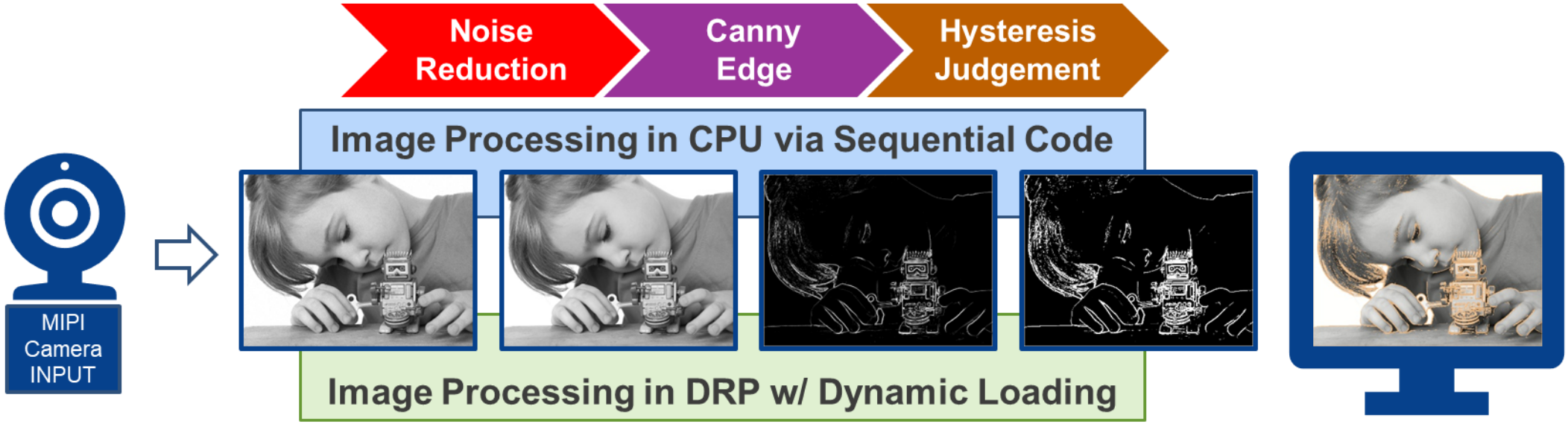
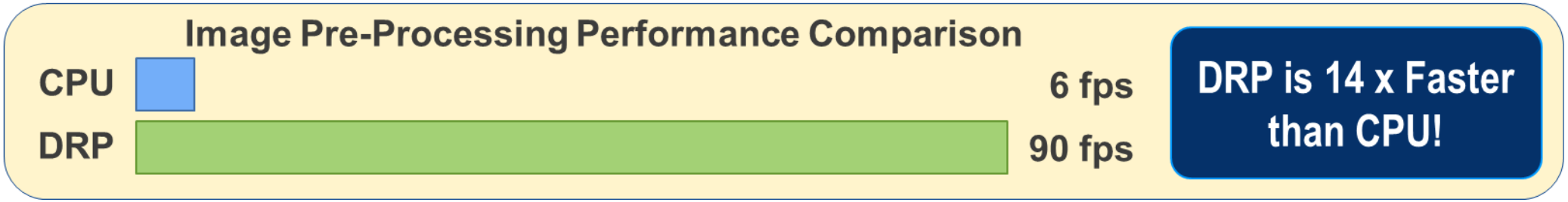




DRP vs. CPU: PERFORMANCE COMPARISON

RZ/A2M MPU WITH DRP TECHNOLOGY

RZ/A2M FOR EMBEDDED REAL TIME IMAGE PROCESSING

Embedded DRP Accelerator

- 10 x the speed of existing CPUs for image pre-processing
- Free DRP libraries for application development

High Capacity Built-in RAM (4 MB)

- Eliminate external DRAM in image-based systems
- Simplifies system design, lowers power consumption, reduces BOM cost

Enhanced Functionality for Vision Applications

- Built-in MIPI-CSI interface for widely available low-cost camera modules
- Image distortion correction hardware Image Renderer (IMR) engine

Vision Applications

Facial Recognition

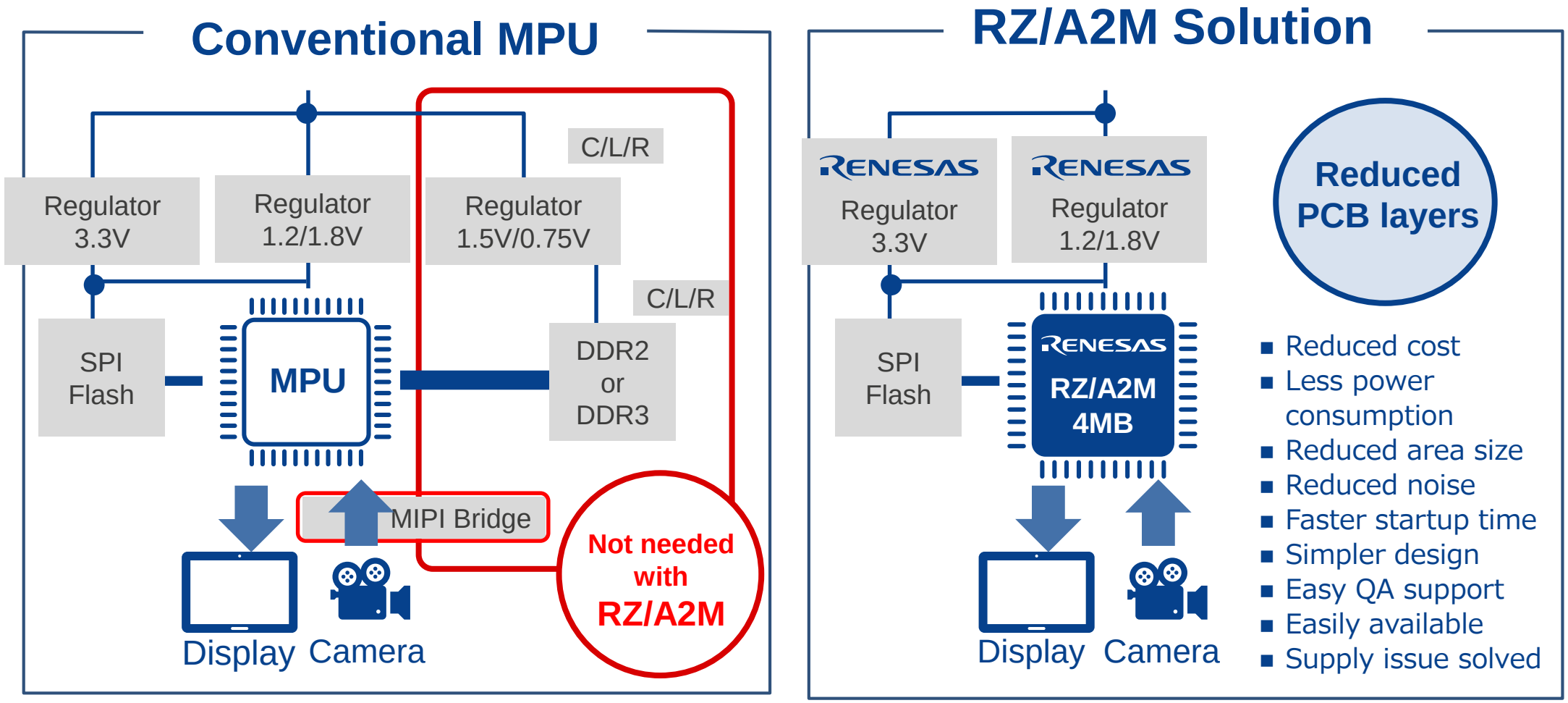
Biometrics

Barcode Scanners

Communication Robots

Home Appliances

RZ/A2M – POWER OF AN MPU, USABILITY OF AN MCU



RZ/A2M MPU

FIRST RZ PRODUCT WITH DRP

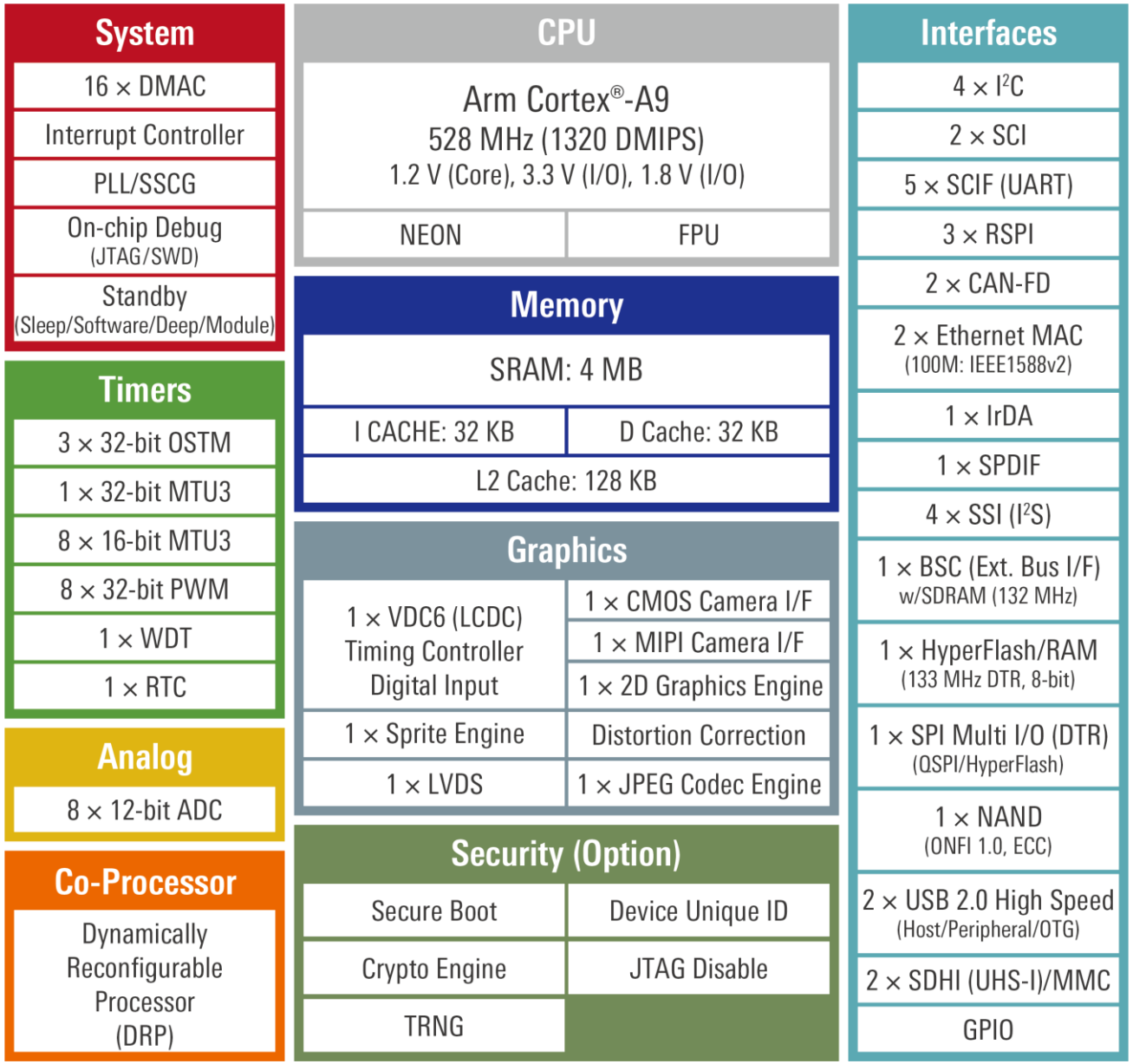
Large 4MB SRAM
- High-speed access, simplified system design, low BOM cost

High performance HMI functions
- Cortex-A9 528MHz with NEON
- 2D Graphics accelerator & Sprite Engine
- MIPI-CSI camera interface
- JPEG Hardware codec

Rich Connectivity
- Dual Ethernet
- USB/SDHI/MMC/NAND
- 8-bit DDR memory interface

High Security
- Trusted Secure IP (TSIP)
- Hardware crypto acceleration
- Key management and storage
- Access management

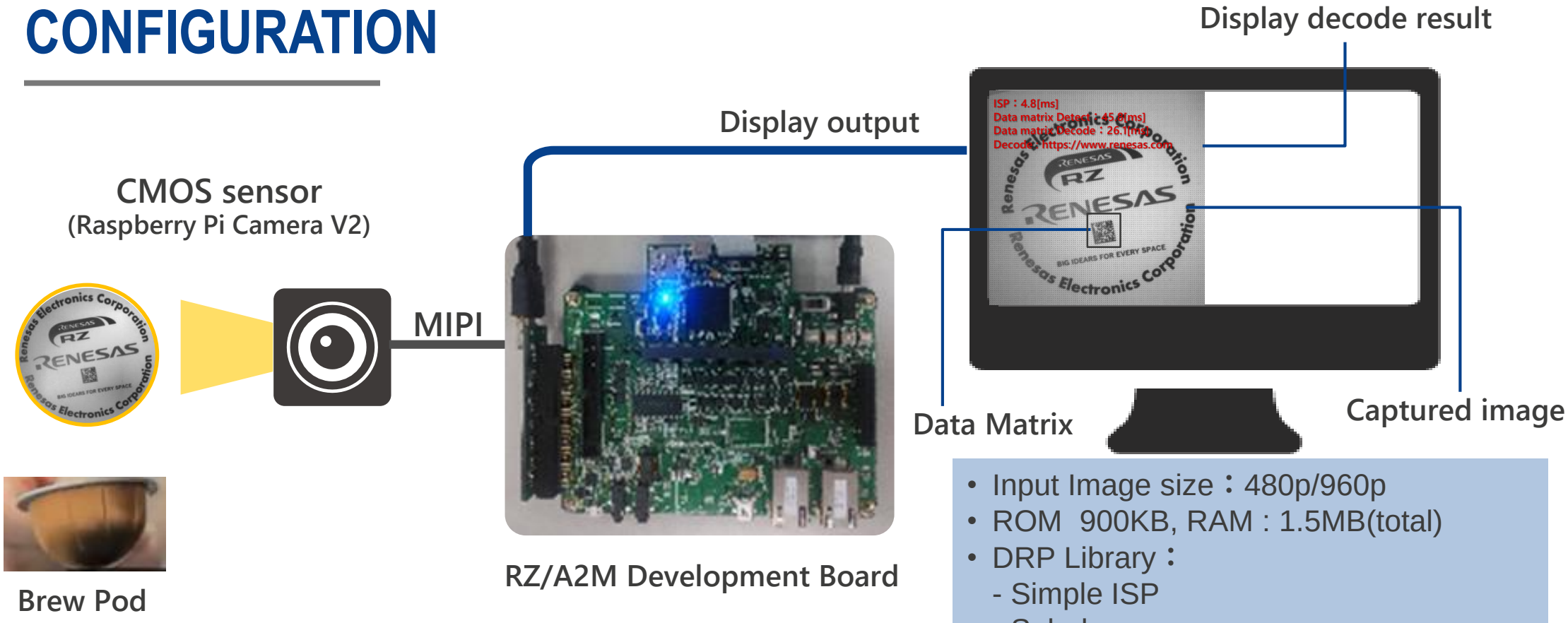
Packages
- 324pin BGA: 19mm/0.8mm pitch
- 272pin BGA : 17mm/0.8mm pitch
- 256pin BGA: 11mm/0.5mm pitch
- 176pin BGA: 13mm/0.8mm pitch



RZ/A2M SOLUTIONS FOR DRP-ACCELERATED IMAGE PROCESSING

OBJECT DETECTION SOLUTION

OBJECT DETECTION DEMO CONFIGURATION



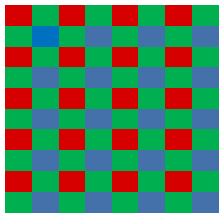
- Input Image size：480p/960p
- ROM 900KB, RAM : 1.5MB(total)
- DRP Library：
  - Simple ISP
  - Sobel
  - Binarization
  - Dilate
  - Erode
  - Find Contour

OBJECT DETECTION EXECUTION

① Data matrix detection processing

DRP-accelerated pre-processing

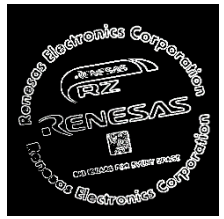
Find areas likely to be data matrix



Input image
480×480

Simple ISP
De-mosaic / Noise reduction / AE control

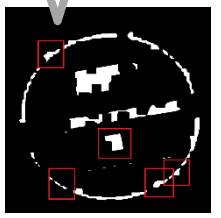
Sobel
Extract contour



Binarization
Data size reduction by binarization

Dilate
Emphasize contour

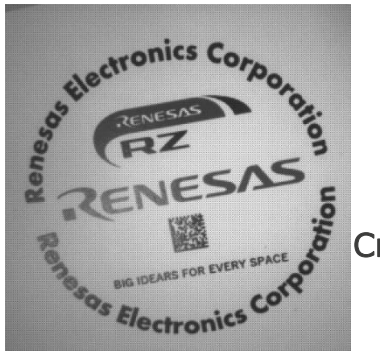
Erode
Remove unnecessary contour



Find Contour
Object detection

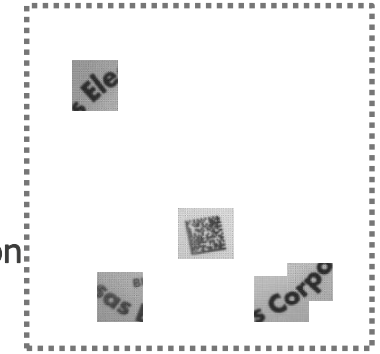
② Data matrix decode processing

Decode cropped areas likely to be data matrix



Input image
960×960

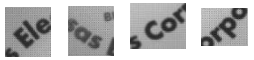
Crop detection areas



Z-Xing (decode processing)

Decode OK

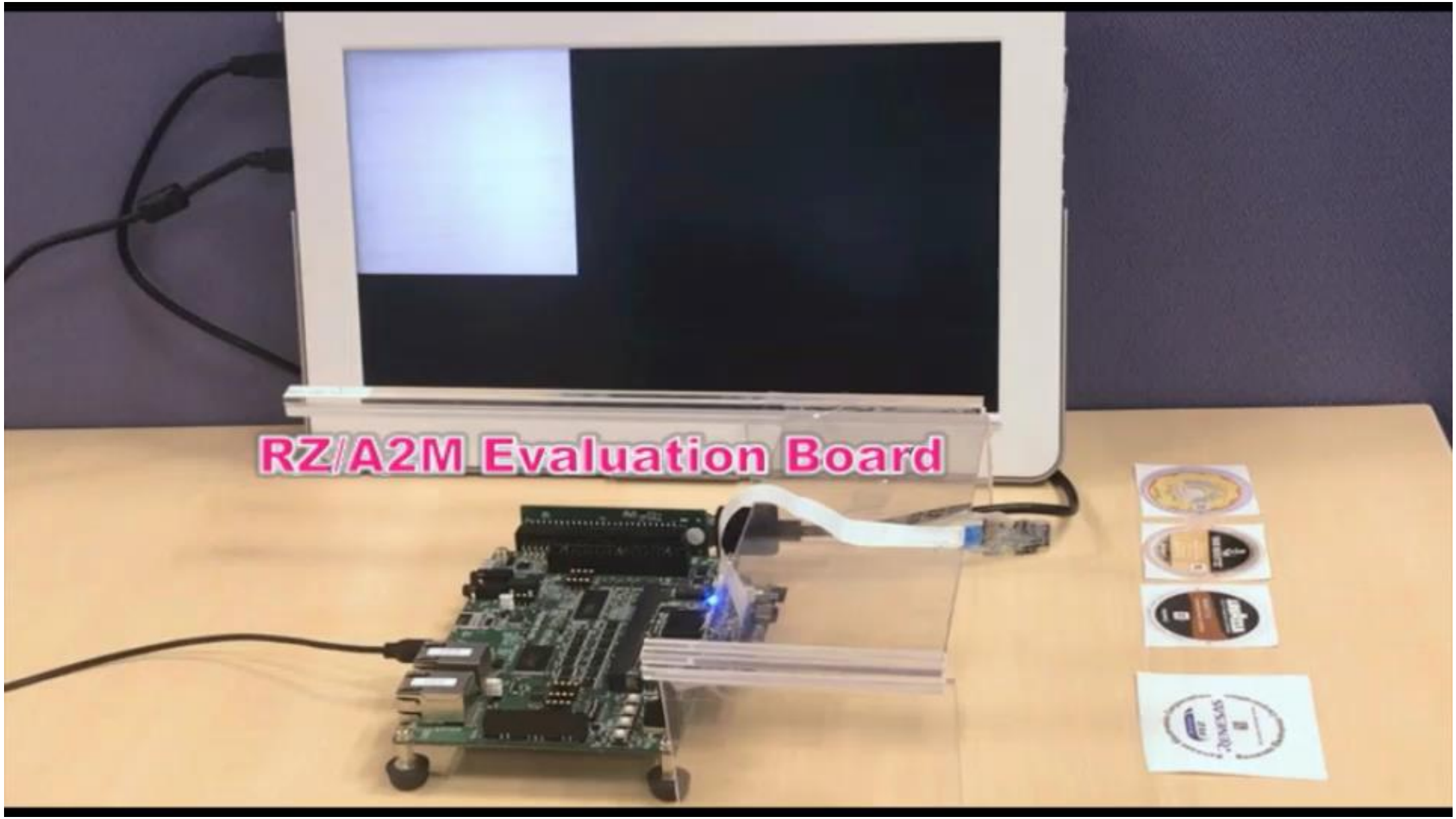
Decode NG



http://renesas.com

Decoding results Display on LCD.

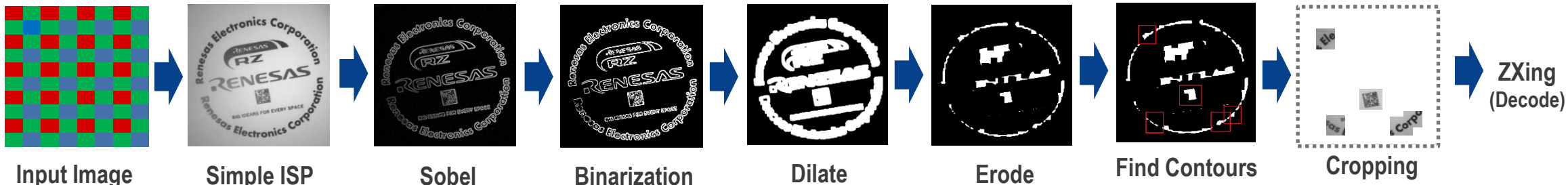
OBJECT DETECTION SOLUTION DEMO



RZ/A2M OBJECT DETECTION SOLUTION

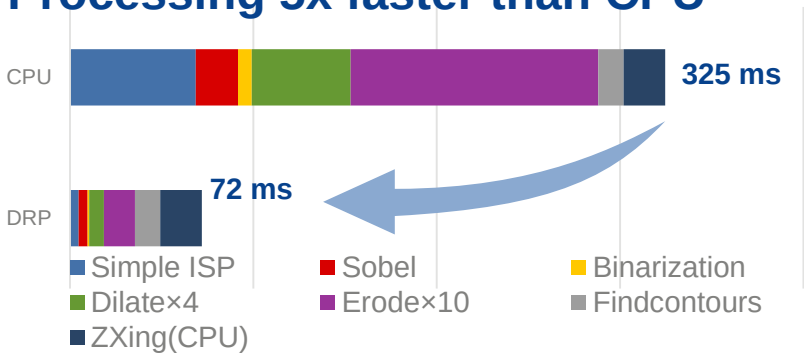
Extracts 2D Barcodes from complex label via DRP library that detects and labels contours in input images

DRP Processing Example



DRP Advantage

Processing 5x faster than CPU



Applications

- Factory inspection
- Home appliances
  (Coffee maker, robot vacuum, microwave oven, etc.)
- Home camera etc.

Design Data

- Free download available now

2D BARCODE SCANNER SOLUTION

2D BARCODE SCANNING

Design Requirements

High-resolution video input

- Easy to scan at a variety of distances
- Adaptable to different environments

Fast scanning and decoding

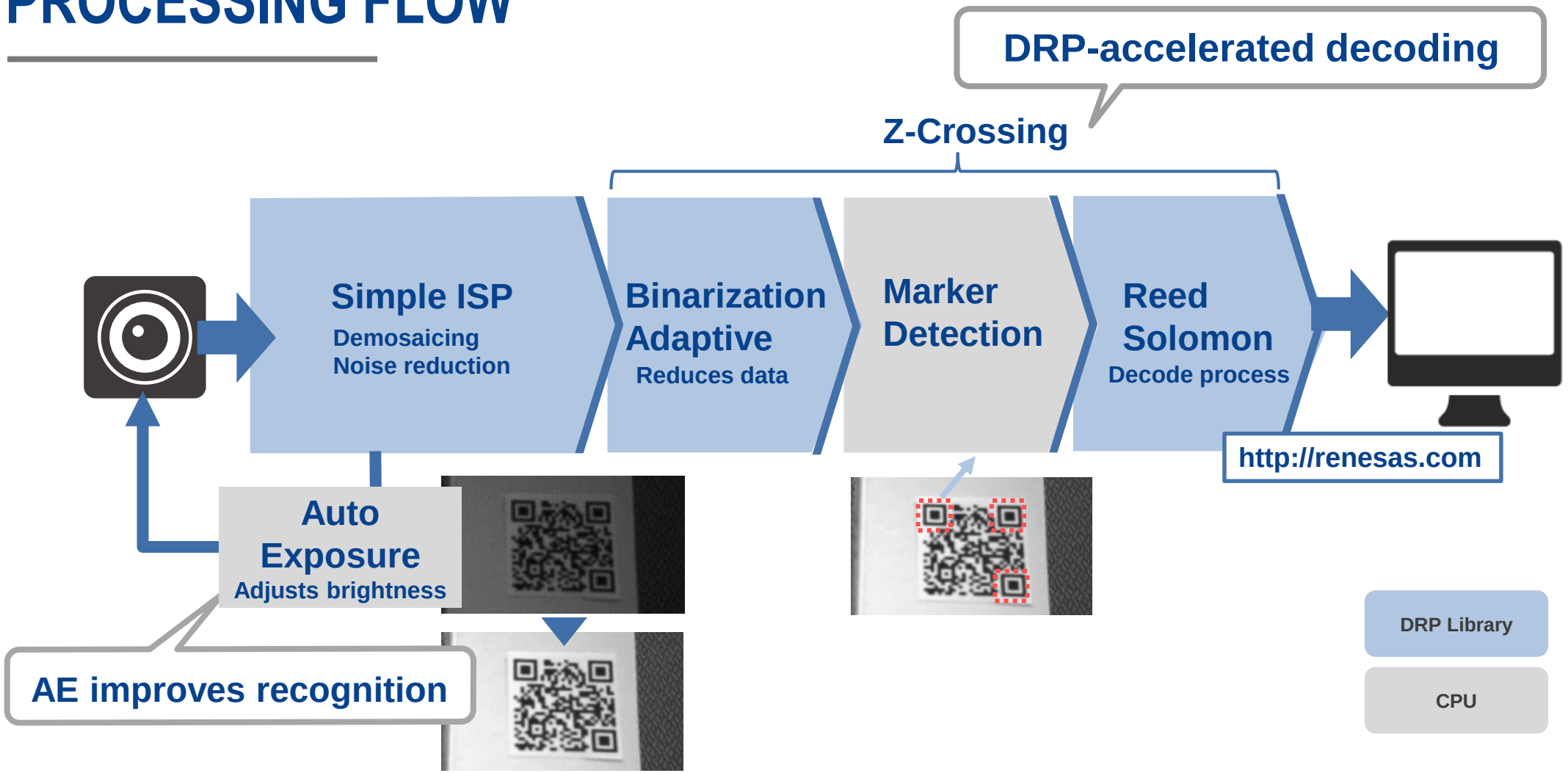
- Improved user experience
- Hi-speed production lines

Low power dissipation

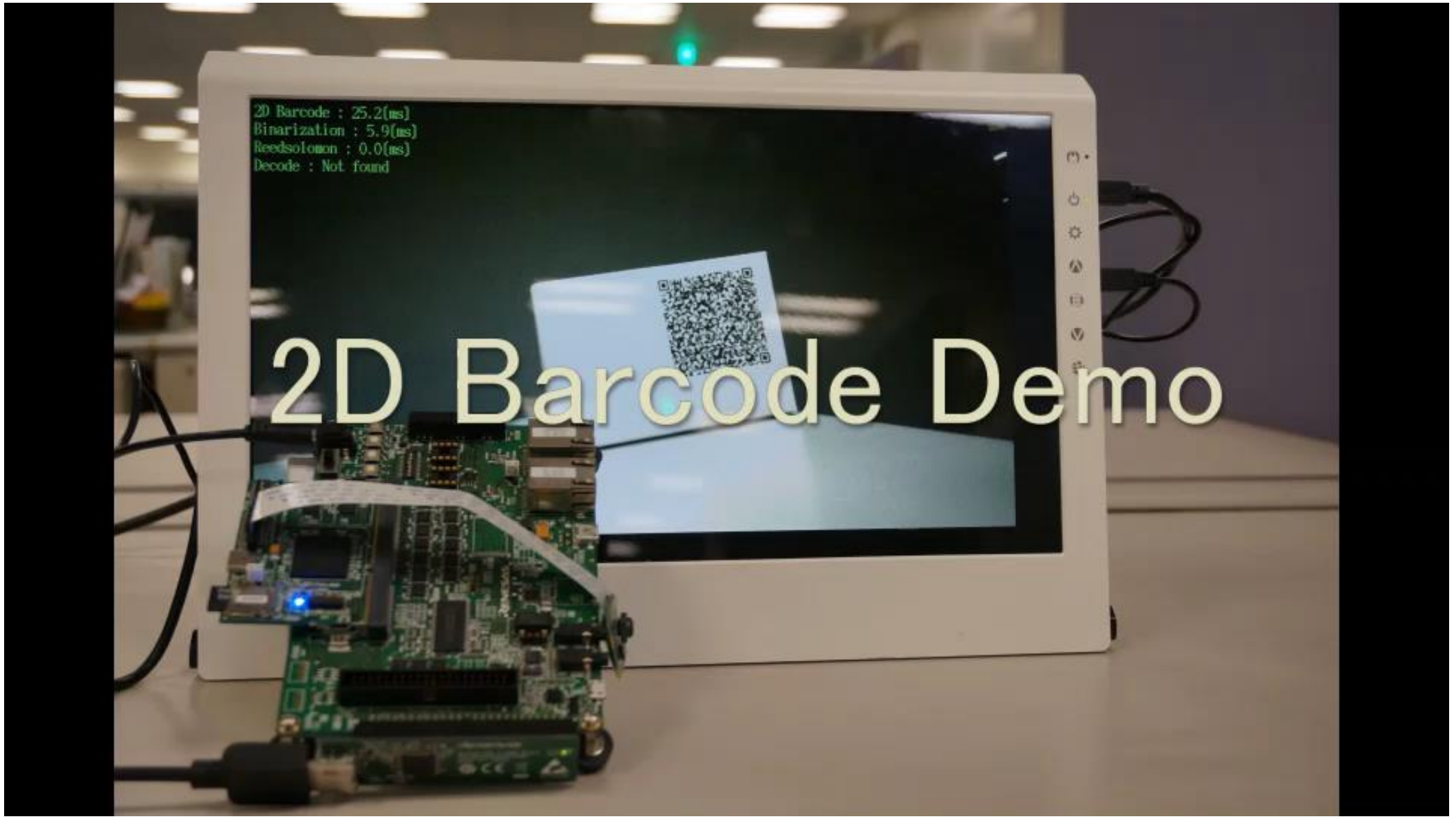
- Battery powered handheld devices
- Sealed enclosures for industrial environments
- Ruggedized enclosures for field deployment

Applications

DRP ACCELERATED 2D BARCODE PROCESSING FLOW



RZ/A2M 2D BARCODE DECODING SOLUTION DEMO

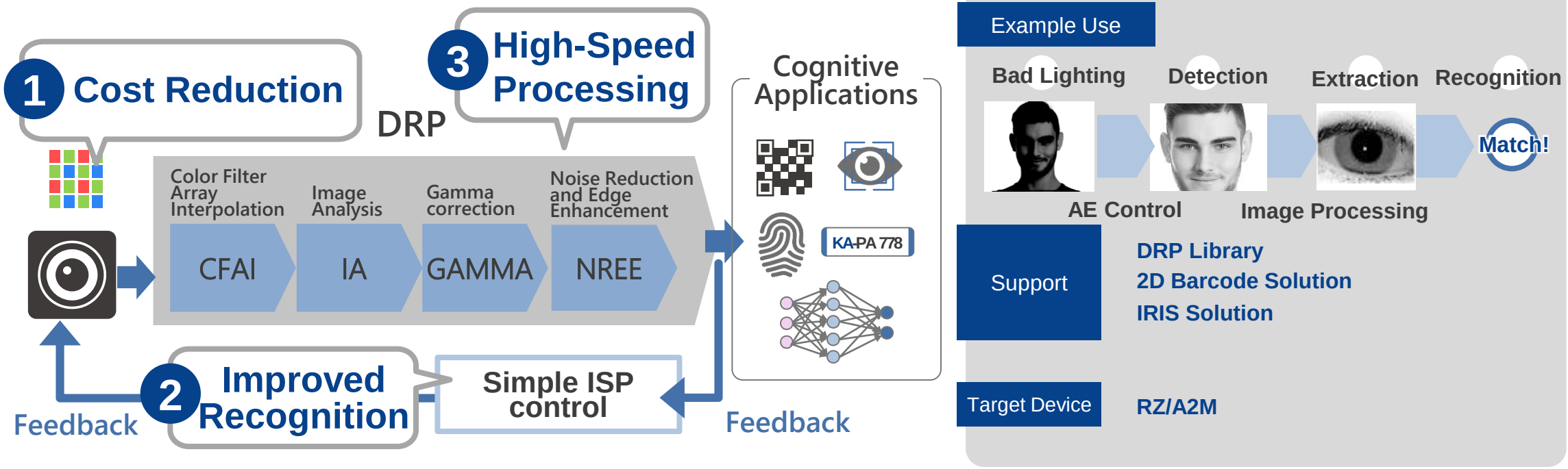


SIMPLE ISP SOLUTION

RZ/A2M SIMPLE ISP

The Simple ISP is a DRP library which works with each solution example for increased value

1. **Cost Reduction:** Using MIPI and Simple ISP, systems can be realized with low-cost CMOS sensors
2. **Improved Recognition:** Increased robustness by combining the ISP and Cognitive-specific AE control
3. **High-speed Processing:** The DRP library accelerates image processing



MOTION DETECTION AND DYNAMIC CONTROL SOLUTION

MOVING OBJECT TRACKING

INTEGRATED VISION AND MOTION PROCESSING

System layered components

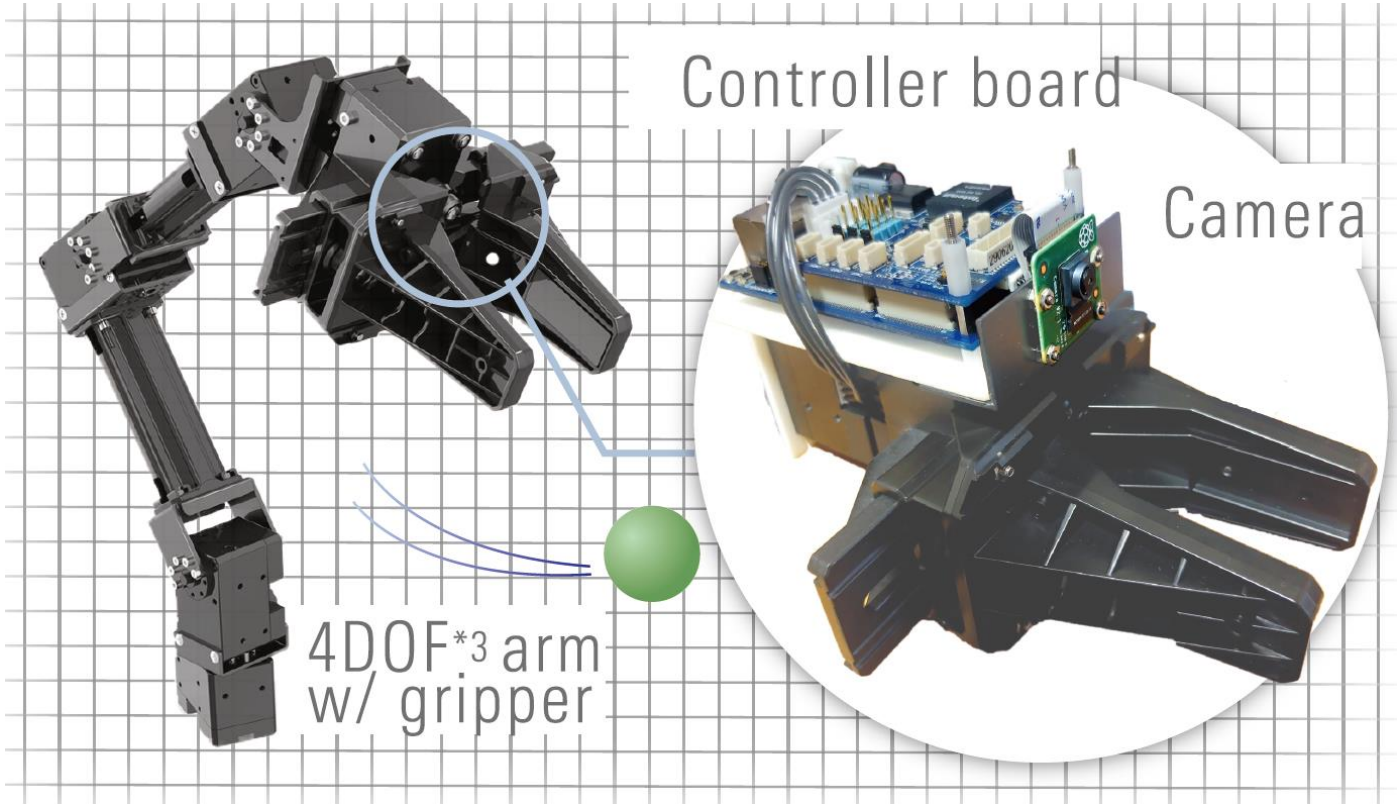
- Application Program
- MIPI® | OpenCV | Dynamics Lib.
- DRP Lib. | FreeRTOS™
- Drivers
- DRP | Arm®Cortex®-A9 | SCI
- RZ/A2M

RZ/A2M DEVELOPMENT BOARD

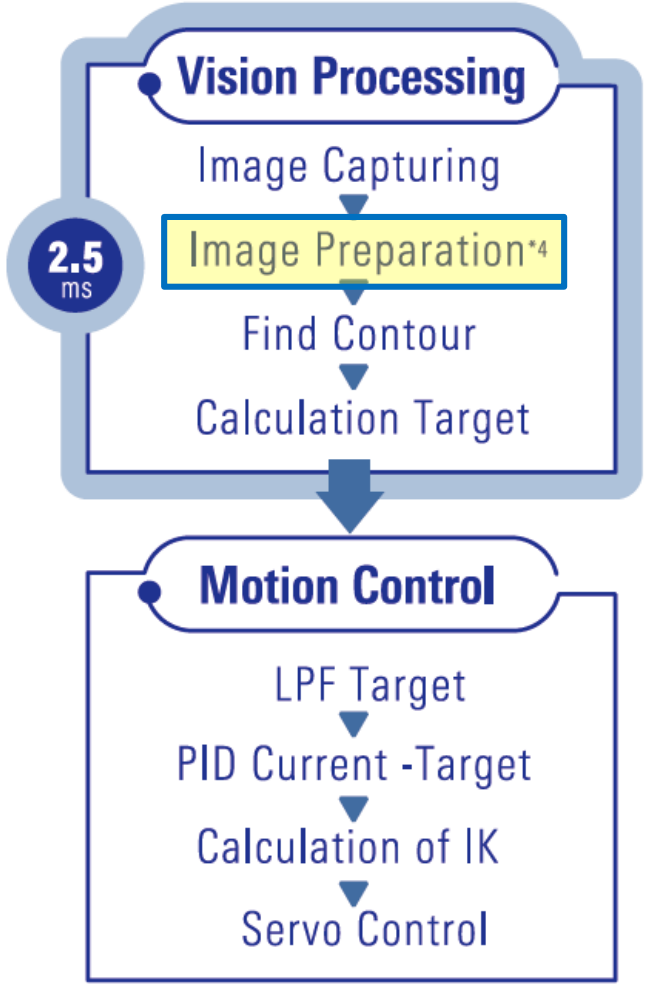
SMALL FORM FACTOR

MOVING OBJECT TRACKING

INTEGRATED VISION AND MOTION PROCESSING



Software flow

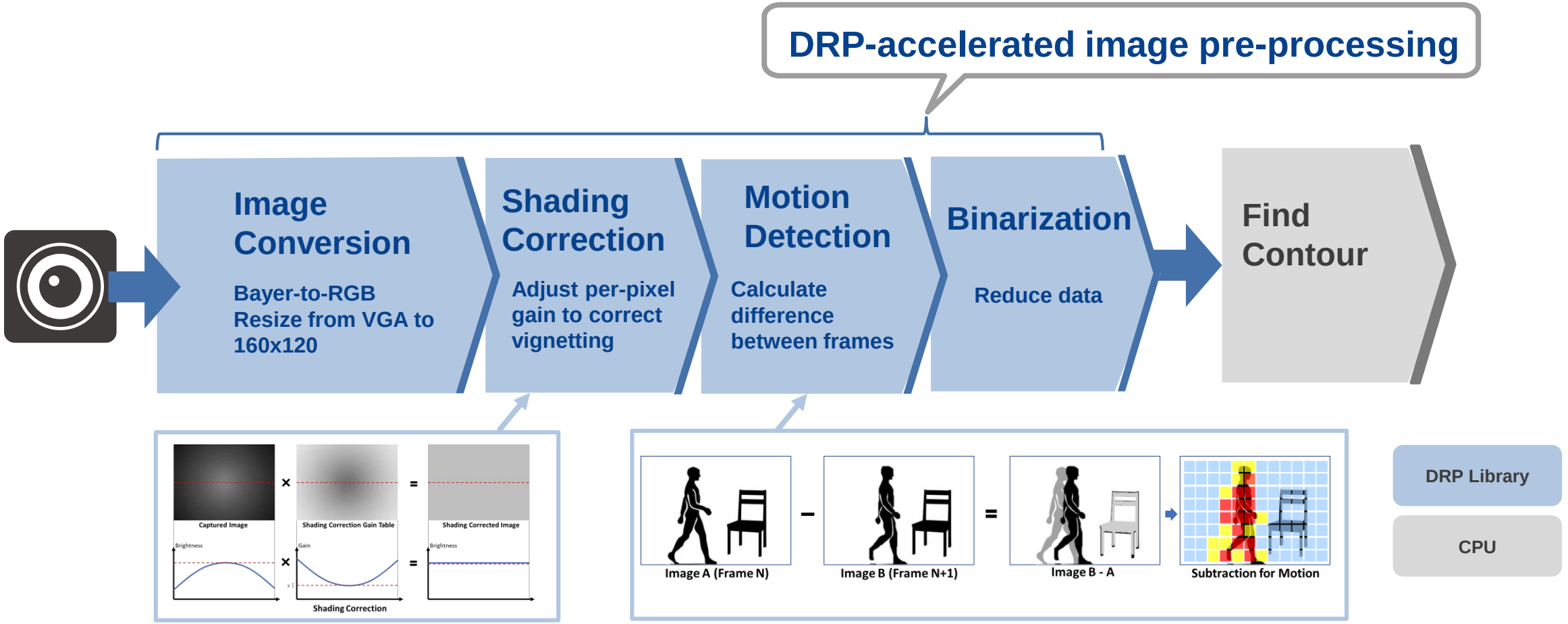


*4 : Image Preparation:Image Conversion + Shading Correction + Subtraction for Motion Detection + Binarization

Robot arm: OpenMANIPULATOR-X (ROBOTIS Co., Ltd.)

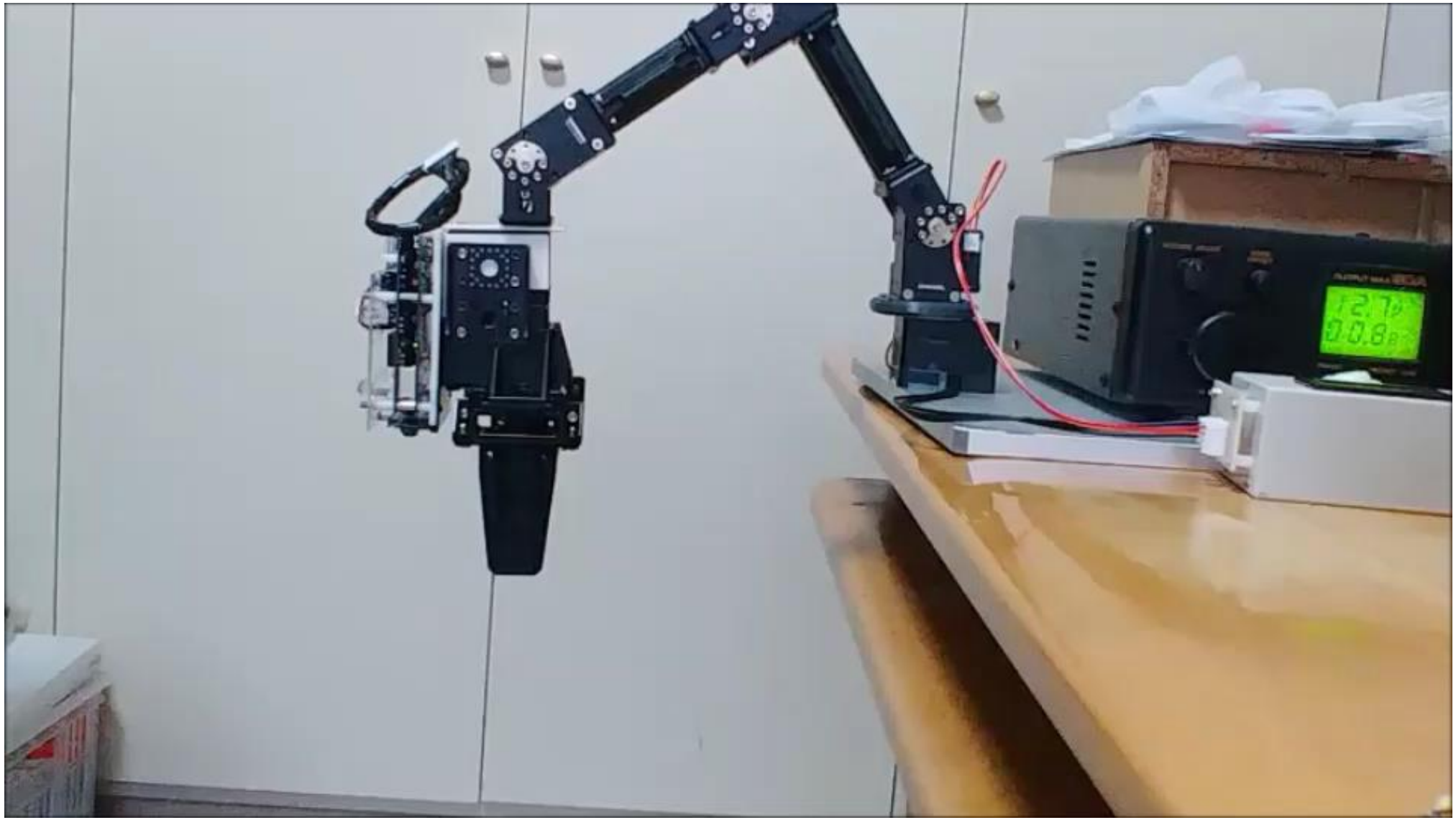
MOVING OBJECT TRACKING

DRP-ACCELERATED VISION PROCESSING FLOW



MOVING OBJECT TRACKING DEMO

INTEGRATED VISION AND MOTION PROCESSING

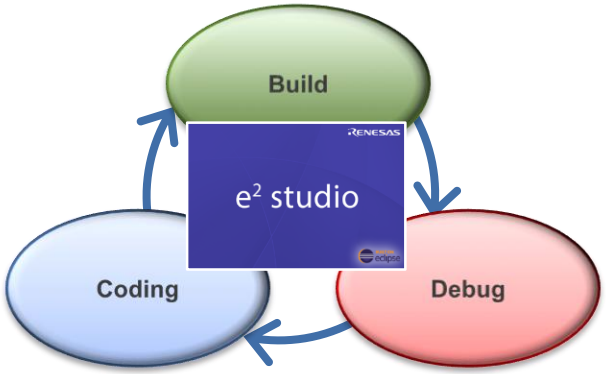


DESIGN RESOURCES FOR RZ/A2M WITH DRP

RZ/A2M DEVELOPMENT ENVIRONMENT OVERVIEW

Development Tools

Integrated Development Environment



Extended interfaces for the IDE to support smart development
- Smart Utilities
- Smart Configurator
- QE (quick and effective tools)

Partner Products

Software

Abundant Sample code

User Application

RZ/A2M Software Package (BSP)

Middleware

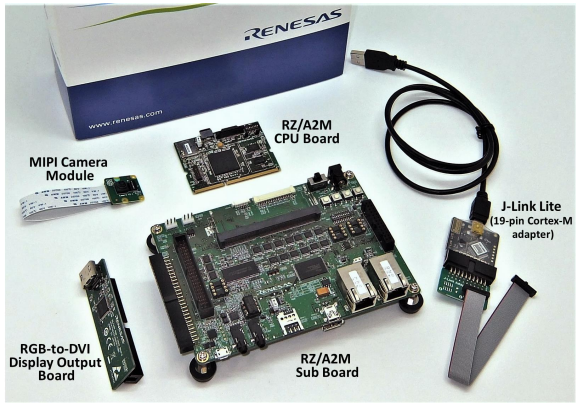
Device Drivers

DRP libraries

Partner Products

Evaluation Boards

Evaluation kit for microprocessors

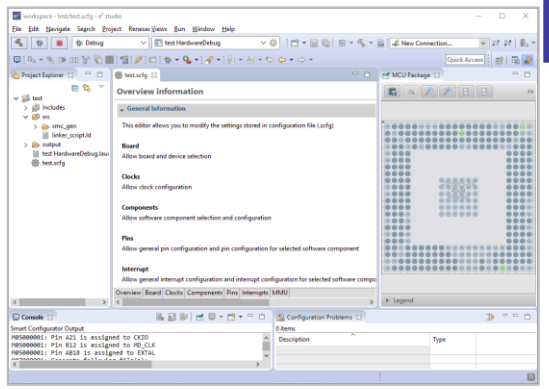


Partner Products

RENESAS TOOLS

Work with Smart Utilities and QE to **improve customer development efficiency** and **shorten development period**

Smart Configurator

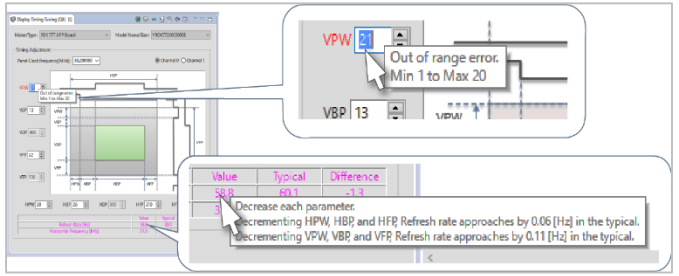


e² studio

Smart Configurator

View memory maps, and configure clock pins and various driver settings through a simple GUI!

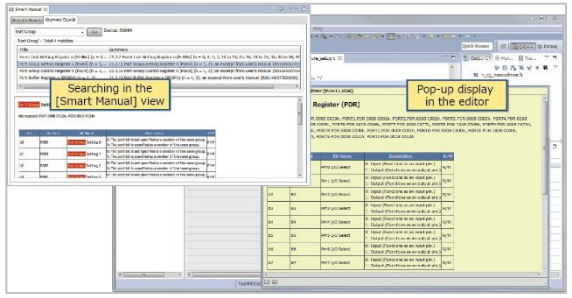
QE



QE for Camera and QE for Display are in planning for the RZ/A2.

Easily-to-use GUI for configuring camera and display timing, adjusting image quality and more!

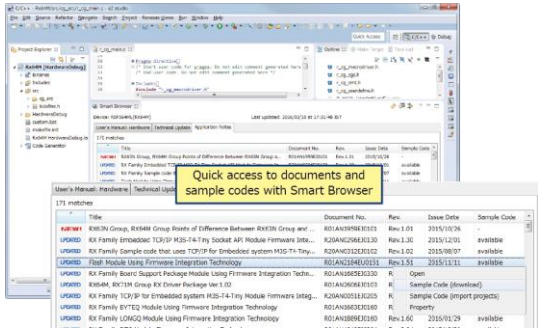
Smart Manual



Using the viewer, you can inspect the manual and look up keywords and register names.

Just by hovering over register and function names with the mouse cursor, the editor displays a pop-up with an explanation of the specification!

Smart Browser

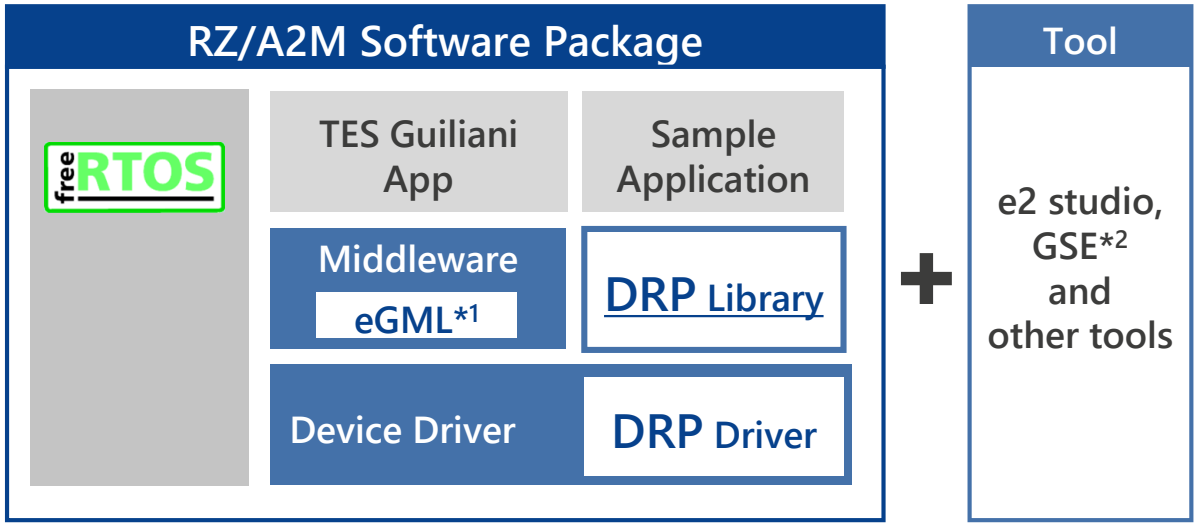


Enables you to look up the latest hardware manuals, technical updates and application notes for your target device.

It's also possible to import projects in order to view sample code, or projects including sample code!

RZ/A2M SOFTWARE PACKAGE

Free **RZ/A2M Software Package**



*1 embedded Graphics Multiplatform Library

*2 Guiliani Streaming Editor

- ✔ **Downloadable** from the Renesas Website
- ✔ Based on **FreeRTOS v10**

IDE	**e2 studio** (Eclipse)
Compiler	GNU Arm Embedded Toolchain 6-2017-q2-update
GUI Tool	TES Guiliani-Lite

Renesas provides various driver samples and applications **to reduce development time**

Target Applications 2D Barcode, Iris Detection ⋯ and more to come !

DRP LIBRARIES

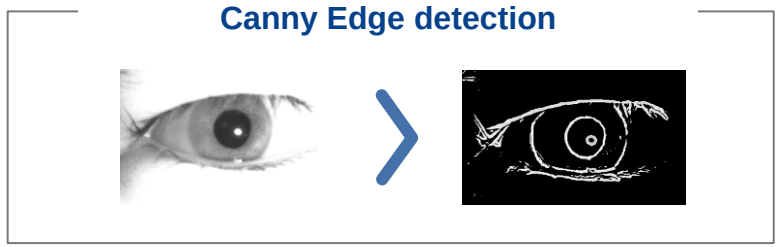
CURRENTLY MORE THAN THIRTY FUNCTIONS AVAILABLE AND MORE ON THE WAY

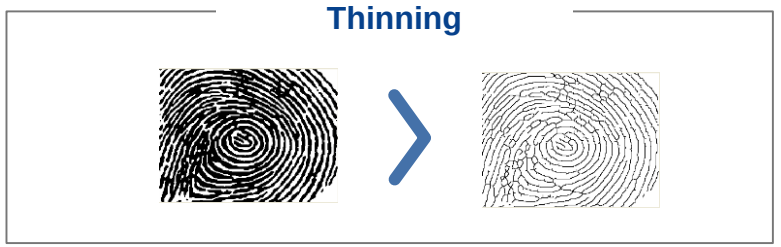
Real Time Camera Image Processing

- Color conversion
- Image filtering
- Geometric transformations
- Image enhancement

Image Recognition

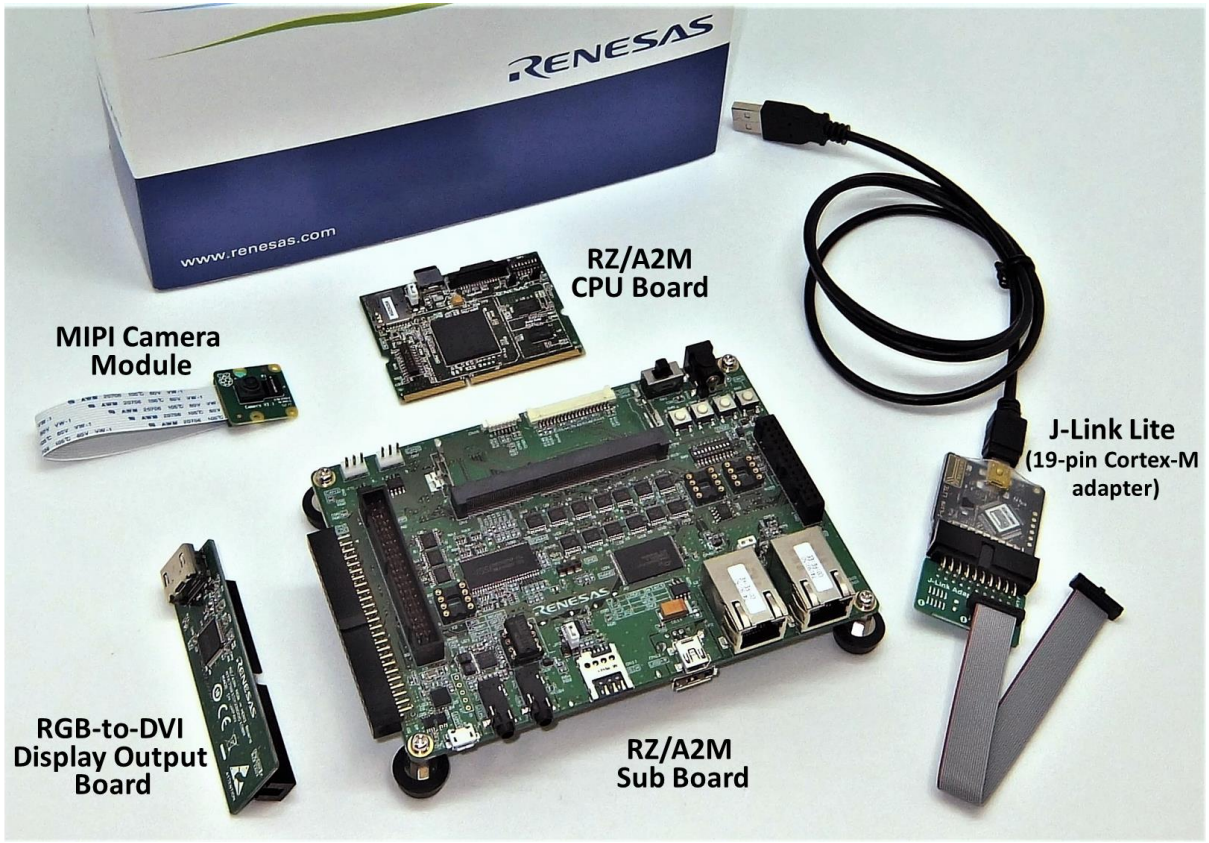
- Feature detection
- Morphological Transformation
- Other (Reed-Solomon error correction)





RZ/A2M EVALUATION KIT

- Complete RZ/A2M Evaluation Platform
- Evaluate DRP technology
- MIPI Camera Module (MIPI CSI)
- HyperFlash™ and HyperRAM™ memory
- RGB conversion board for HDMI display
- Two Ethernet communication channels
- Other peripheral functions: SDHI, USB, etc.
- Segger J-Link Lite debugger



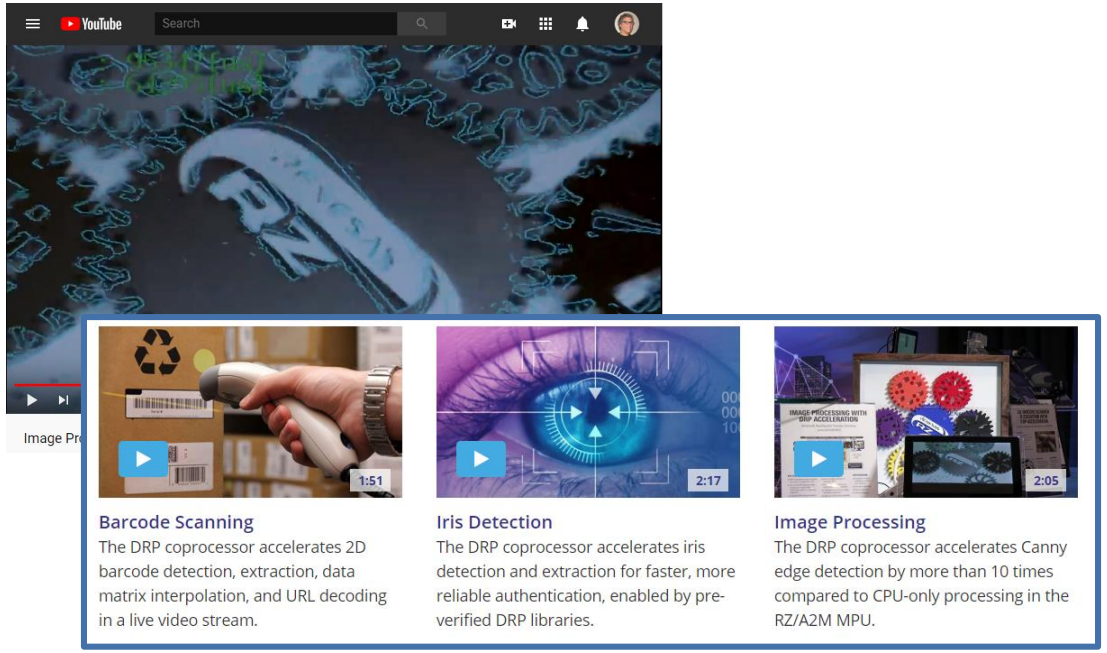
Part number: RTK7921053S00000BE

DRP TECHNOLOGY RESOURCES

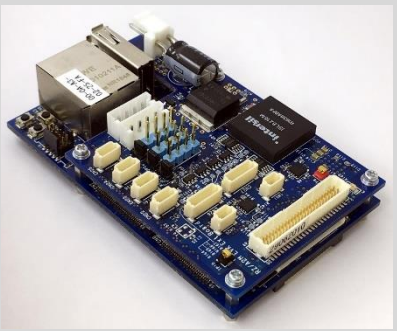
Visit RZ/A2M MPU Product Page

- **Watch** Videos: RZ/A2 MPU Overview; DRP Technology Overview; DRP Solution Demos
- **Download** Free Development Tools
- **Download** Free RZA2M Software Package
- **Download** Free RZA2M Demo Designs and Application Guides
- **Buy** RZ/A2M Evaluation Kit

https://www.renesas.com/rza2m



RZ/A2M Eva-Lite



SHIMAFUJI

http://www.shimafuji.co.jp/en/products/1522

SUMMARY AND NEXT STEPS

- Embedded Vision Evolution demands more computing power
- Limitations of available architectures: scalability, power consumption, flexibility, and efficiency
- DRP technology addresses these challenges:
  - Massively-parallel custom-configured pipelined hardware data path
  - Virtually expandable silicon via time domain multiplexing (dynamic reconfiguration)
- DRP-based solutions accelerate image processing, reduce power, and reduce cost
- Renesas continues investment in DRP technology to enhance additional applications

THANK YOU

Empowering Product Creators to Harness Embedded Vision

The Embedded Vision Alliance (www.Embedded-Vision.com) is a partnership of 90+ leading embedded vision technology and services suppliers, and solutions providers

Mission: Inspire and empower product creators to incorporate visual intelligence into their products

The Alliance provides low-cost, high-quality technical educational resources for product developers

Register for updates at www.Embedded-Vision.com

The Alliance enables vision technology providers to grow their businesses through leads, ecosystem partnerships, and insights

For membership, email us: membership@Embedded-Vision.com

Join us at the Embedded Vision Summit
May 18-21, 2020—Santa Clara, California

The only industry event focused on enabling product creators to create "machines that see"

- *"Awesome! I was very inspired!"*
- *"Fantastic. Learned a lot and met great people."*
- "*Wonderful speakers and informative exhibits!*"

Embedded Vision Summit 2020 highlights:

- **Inspiring keynotes** by leading innovators
- High-quality, practical **technical, business and product talks**
- Exciting **demos** of the latest apps and technologies

Visit www.EmbeddedVisionSummit.com to sign up for updates